第四讲　系统时钟

主讲：叶剑
电话：13728639620
Email：yejian@hit.edu.cn

第四讲：系统时钟

1、OSC和PLL模块

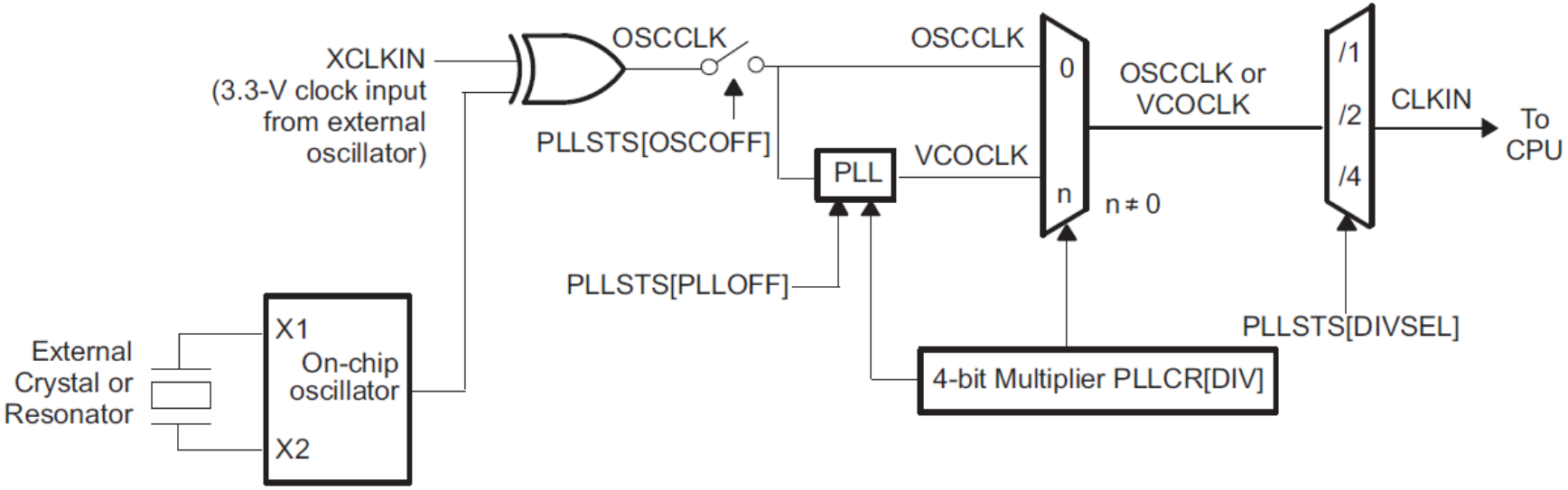
2、外设时钟信号

3、低功耗模式

4、Watchdog看门狗模块

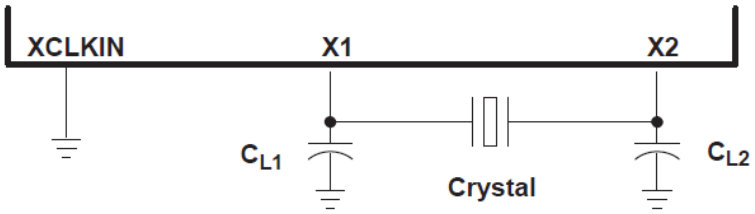
5、CPU定时器0/1/2

OSC三种时钟方案

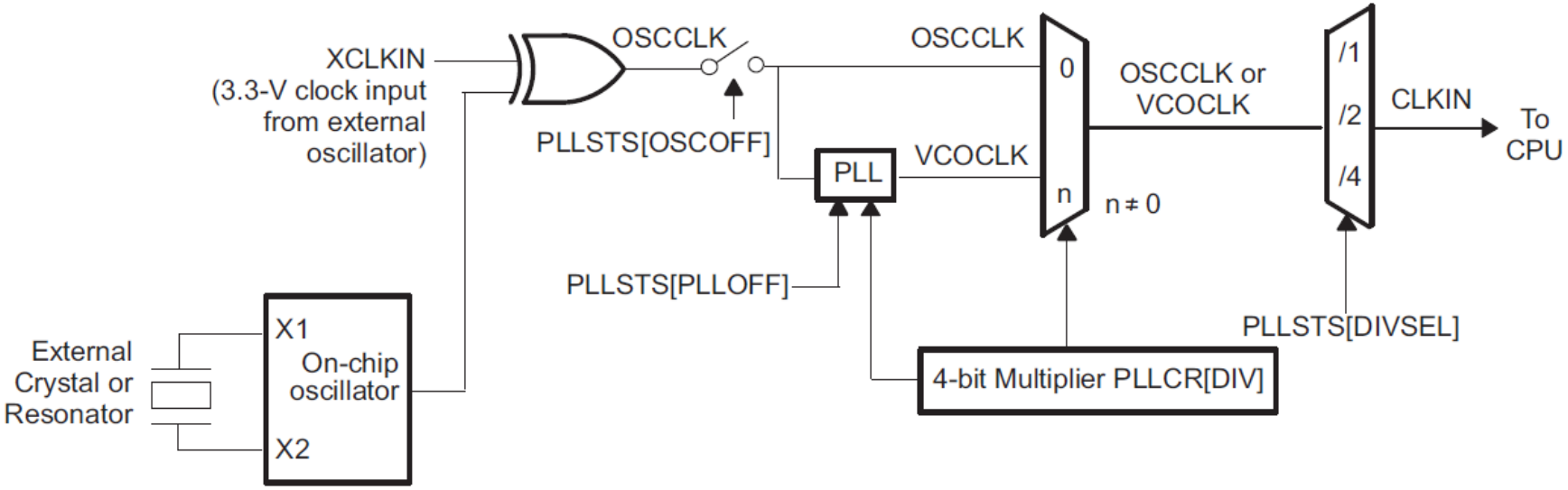


- **Crystal/Resonator Operation:**

  The on-chip oscillator enables the use of an external crystal/resonator to be attached to the device to provide the time base to the device. The crystal/resonator is connected to the X1/X2 pins and XCLKIN is tied low.



OSC三种时钟方案



- **External clock source operation:**

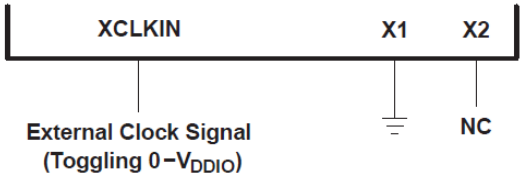
  If the on-chip oscillator is not used, this mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on either the X1 or the XCLKIN pin.

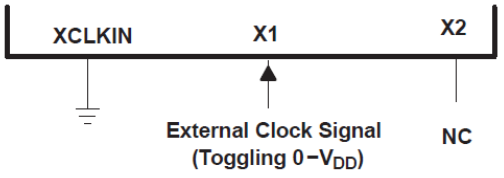
  Option 1: External clock on the XCLKIN pin:

  When using XCLKIN as the external clock source, you must tie X1 low and leave X2 disconnected. In this case, an external oscillator clock is connected to the XCLKIN pin, which allows for a 3.3-V clock source to be used.

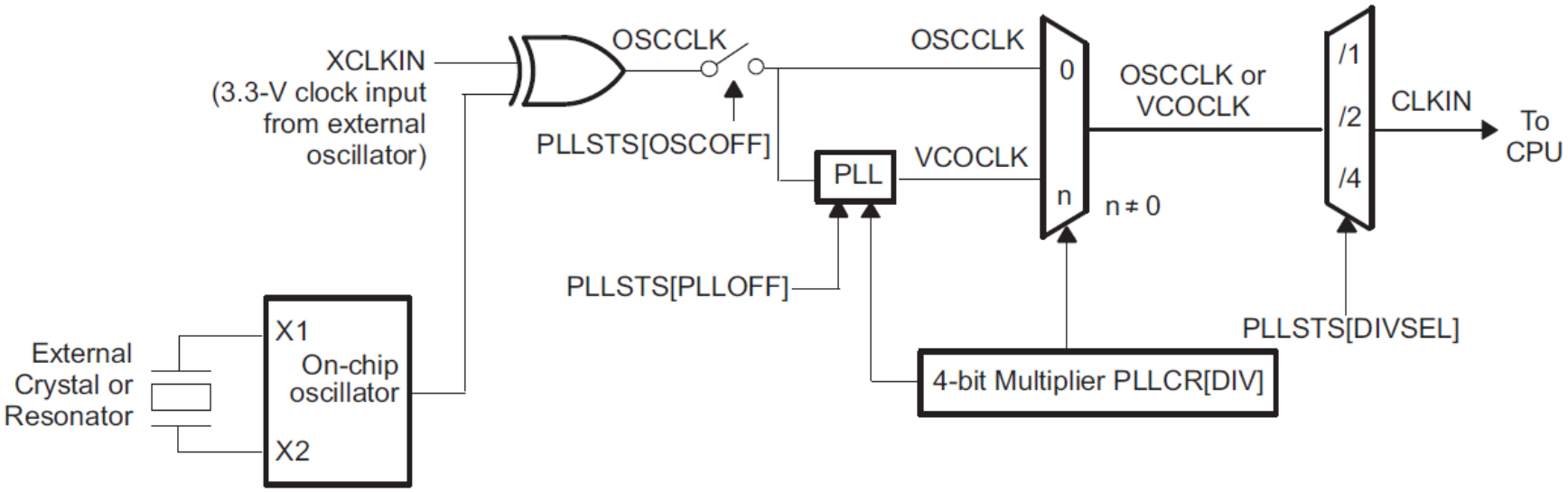
  Option 2: External clock on the X1 pin:

  When using X1 as the clock source, you must tie XCLKIN low and leave X2 disconnected. In this case, an external oscillator clock is connected to the X1 pin, which allows for a 1.8-V clock source to be used.





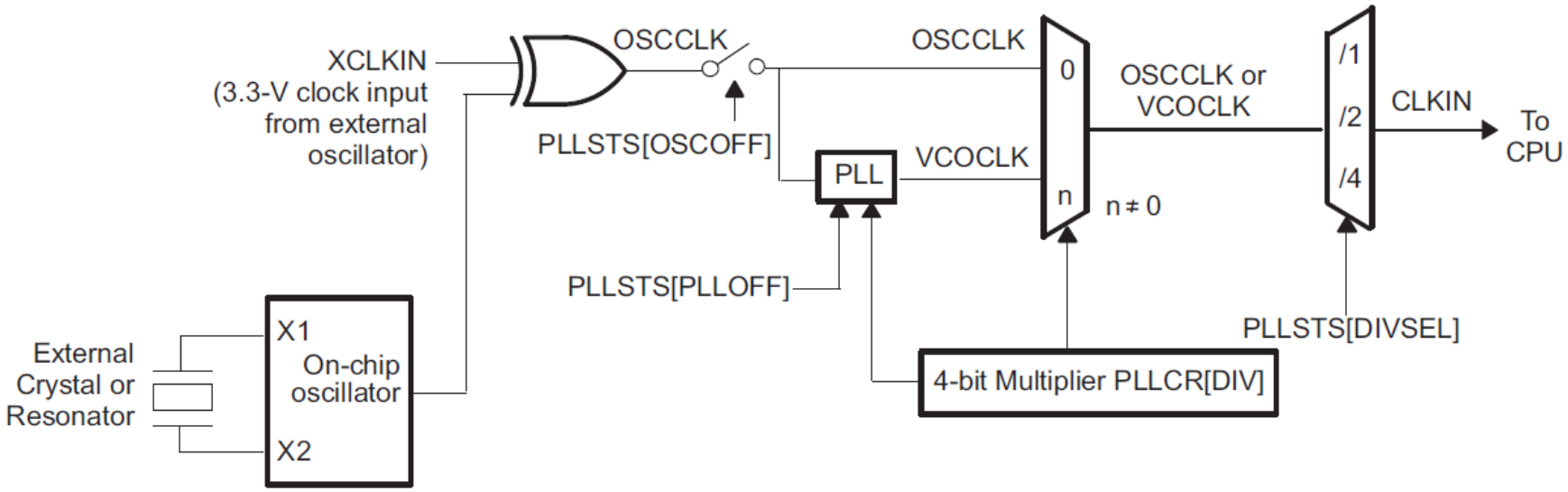
PLL模块



◆PLL倍频时一定要分频，不倍频时才允许不分频。

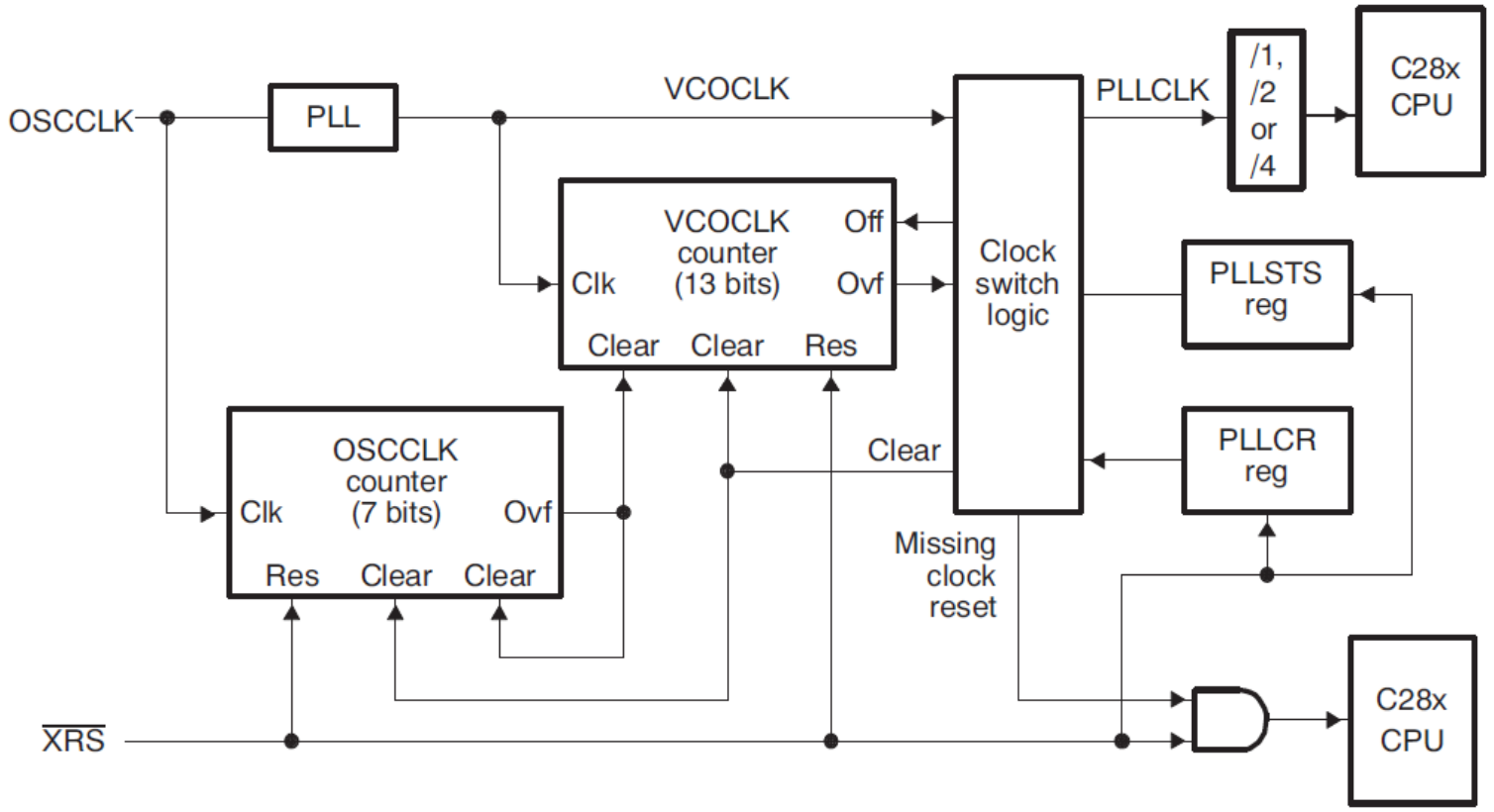
PLL Mode	Remarks	PLLSTS[DIVSEL] (1)	SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Enabled	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR, the device will switch to PLL Bypass mode until the PLL locks.	0, 1 2	OSCCLK*n/4 OSCCLK*n/2

PLL模块



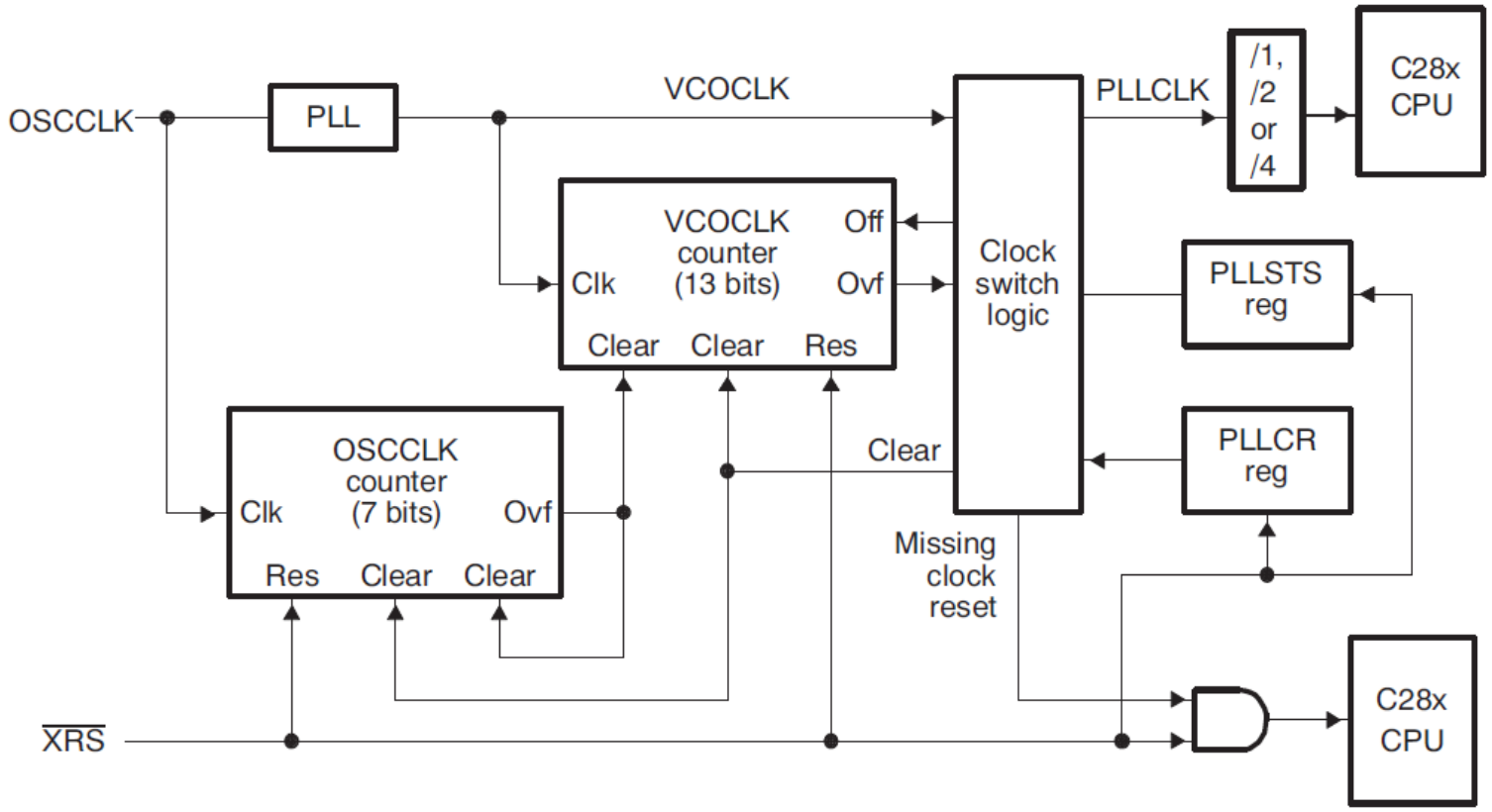
	SYSCLKOUT (CLKIN) [2]		
PLLCR[DIV] Value [3]	**PLLSTS[DIVSEL] = 0 or 1**	**PLLSTS[DIVSEL] = 2**	**PLLSTS[DIVSEL] = 3**
0000 (PLL bypass)	OSCCLK/4 (Default)	OSCCLK/2	OSCCLK
0001	(OSCCLK * 1)/4	(OSCCLK*1)/2	–
0010	(OSCCLK * 2)/4	(OSCCLK*2)/2	–
0011	(OSCCLK * 3)/4	(OSCCLK*3)/2	–
0100	(OSCCLK * 4)/4	(OSCCLK*4)/2	–
0101	(OSCCLK * 5)/4	(OSCCLK*5)/2	–
0110	(OSCCLK * 6)/4	(OSCCLK*6)/2	–
0111	(OSCCLK * 7)/4	(OSCCLK*7)/2	–
1000	(OSCCLK * 8)/4	(OSCCLK*8)/2	–
1001	(OSCCLK * 9)/4	(OSCCLK*9)/2	–
1010	(OSCCLK * 10)/4	(OSCCLK*10)/2	–
1011 - 1111	Reserved	Reserved	Reserved

时钟信号监视电路



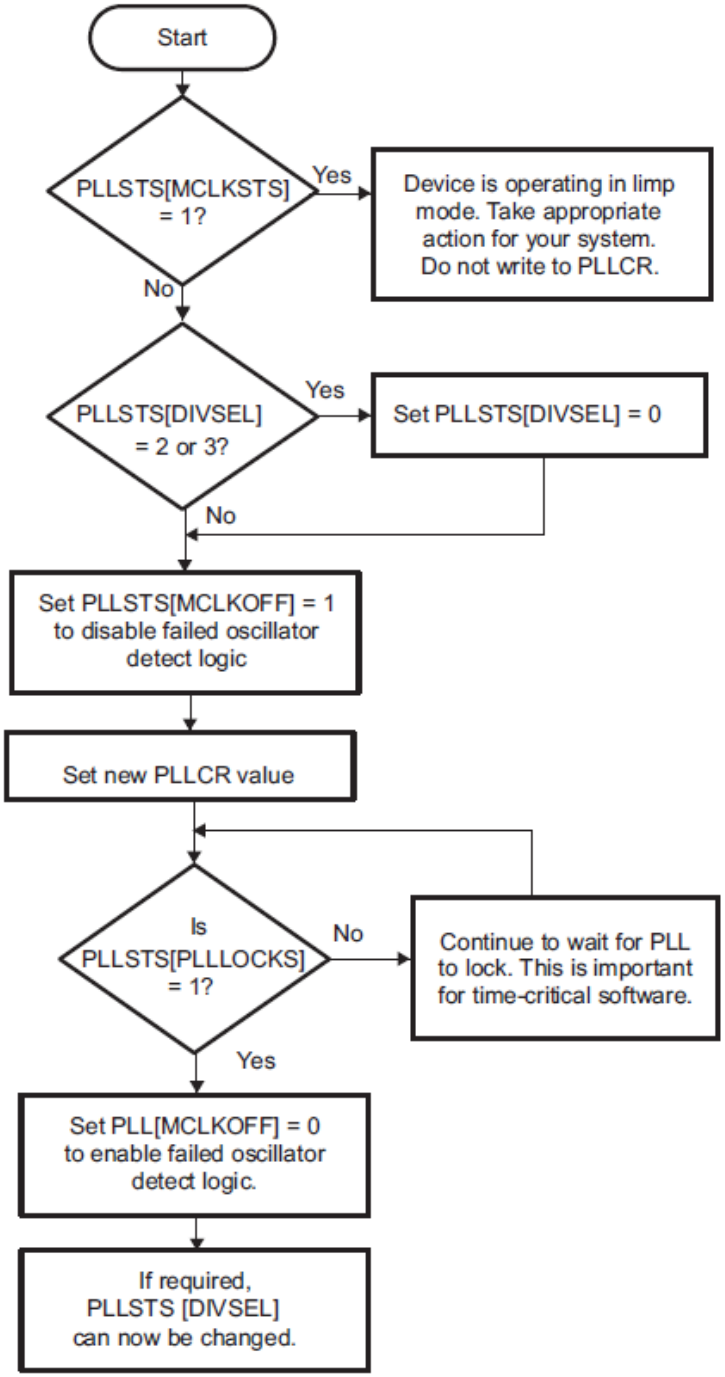
PARAMETER				MIN	TYP	MAX	UNIT
f_x	Input clock frequency	Resonator (X1/X2)		20		35	MHz
		Crystal (X1/X2)		20		35	
		External oscillator/clock source (XCLKIN or X1 pin)	150-MHz device	4		150	
			100-MHz device	4		100	
f_l	Limp mode SYSCLKOUT frequency range (with /2 enabled)				1 - 5		MHz

时钟信号监视电路



3	MCLKSTS		Missing Clock Status Bit. Check the status of this bit after a reset to determine whether a missing oscillator condition was detected. Under normal conditions, this bit should be 0. Writes to this bit are ignored. This bit will be cleared by writing to the MCLKCLR bit or by forcing an external reset.
		0	Indicates normal operation. A missing clock condition has not been detected.
		1	Indicates that OSCCLK was detected as missing. The main oscillator fail detect logic has reset the device and the CPU is now clocked by the PLL operating at the limp mode frequency.

配置PLLCR寄存器


Start
PLLSTS[MCLKSTS] = 1?
Yes
Device is operating in limp mode. Take appropriate action for your system. Do not write to PLLCR.
No
PLLSTS[DIVSEL] = 2 or 3?
Yes
Set PLLSTS[DIVSEL] = 0
No
Set PLLSTS[MCLKOFF] = 1 to disable failed oscillator detect logic
Set new PLLCR value
Is PLLSTS[PLLLOCKS] = 1?
No
Continue to wait for PLL to lock. This is important for time-critical software.
Yes
Set PLL[MCLKOFF] = 0 to enable failed oscillator detect logic.
If required, PLLSTS [DIVSEL] can now be changed.

第四讲：系统时钟

1、OSC和PLL模块

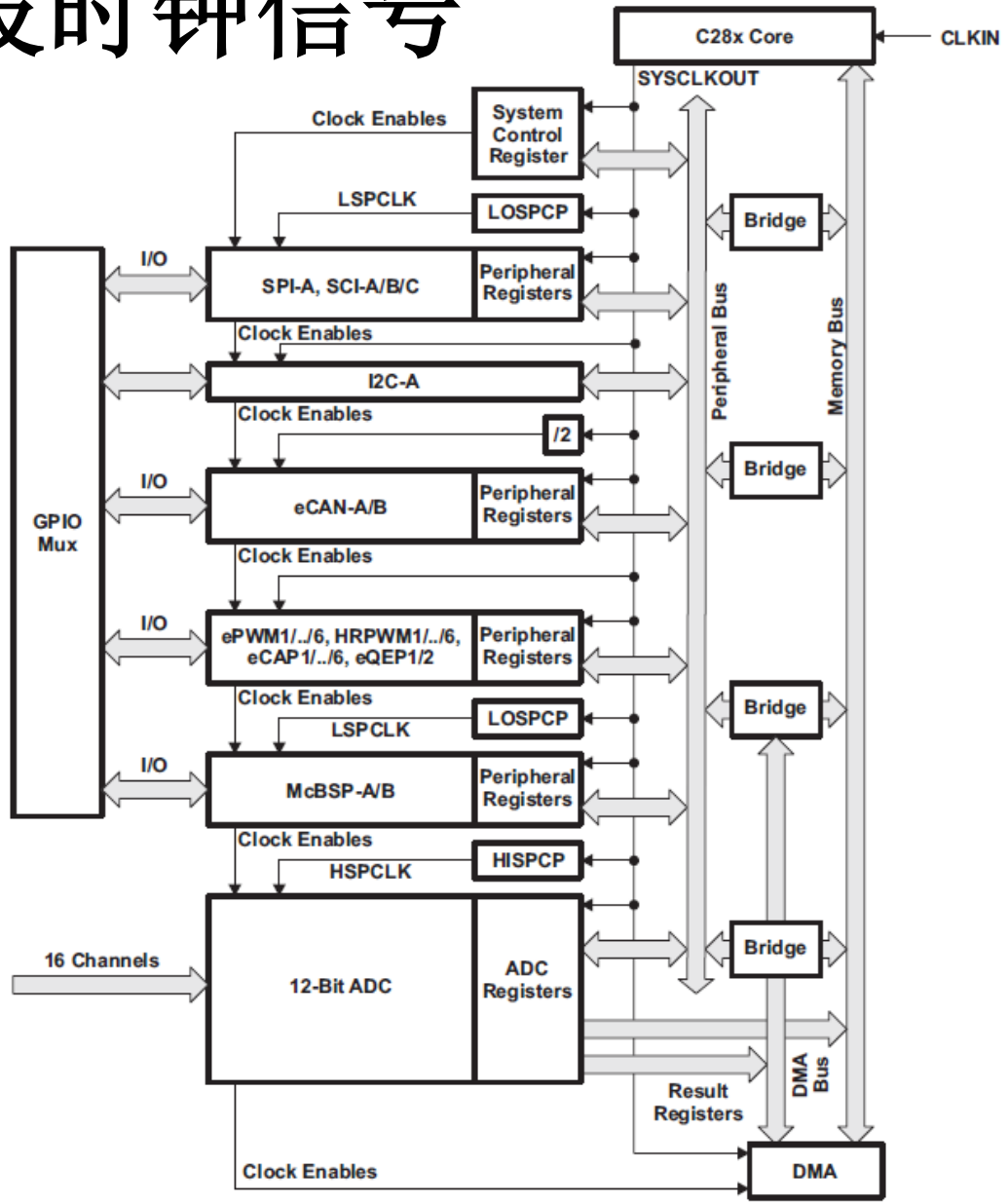
2、外设时钟信号

3、低功耗模式

4、Watchdog看门狗模块

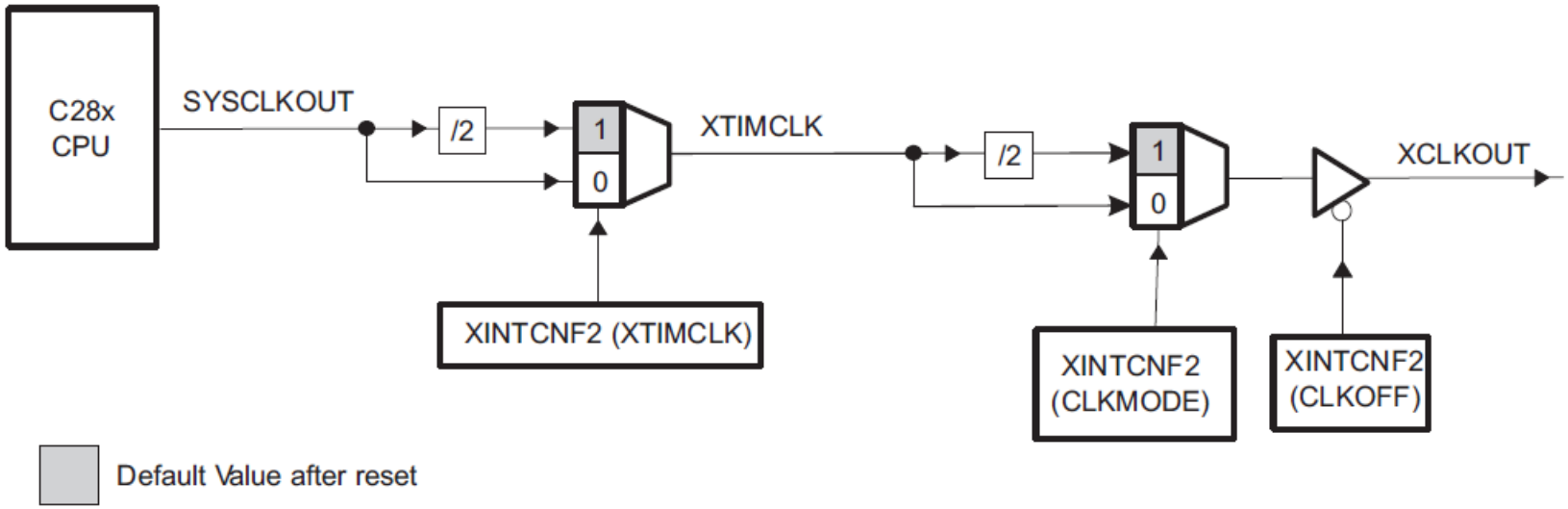
5、CPU定时器0/1/2

片内外设时钟信号



A CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

片外时钟信号XCLKOUT



◆XCLKOUT can be either equal to, one-half, or one-fourth of SYSCLKOUT.

第四讲：系统时钟

1、OSC和PLL模块

2、外设时钟信号

3、低功耗模式

4、Watchdog看门狗模块

5、CPU定时器0/1/2

低功耗模式

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On(2)	$\overline{\text{XRS}}$, Watchdog interrupt, any enabled interrupt, XNMI
STANDBY	01	On (watchdog still running)	Off	Off	$\overline{\text{XRS}}$, Watchdog interrupt, GPIO Port A signal, debugger(3), XNMI
HALT	1X	Off (oscillator and PLL turned off, watchdog not functional)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A signal, XNMI, debugger(3)

(1) The Exit column lists which signals or under what conditions the low power mode will be exited. A low signal, on any of the signals, will exit the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode will not be exited and the device will go back into the indicated low power mode.

(2) The IDLE mode on the C28x behaves differently than on the 24x/240x. On the C28x, the clock output from the CPU (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.

(3) On the C28x, the JTAG port can still function even if the CPU clock (CLKIN) is turned off.

第四讲：系统时钟

1、OSC和PLL模块

2、外设时钟信号

3、低功耗模式

4、Watchdog看门狗模块

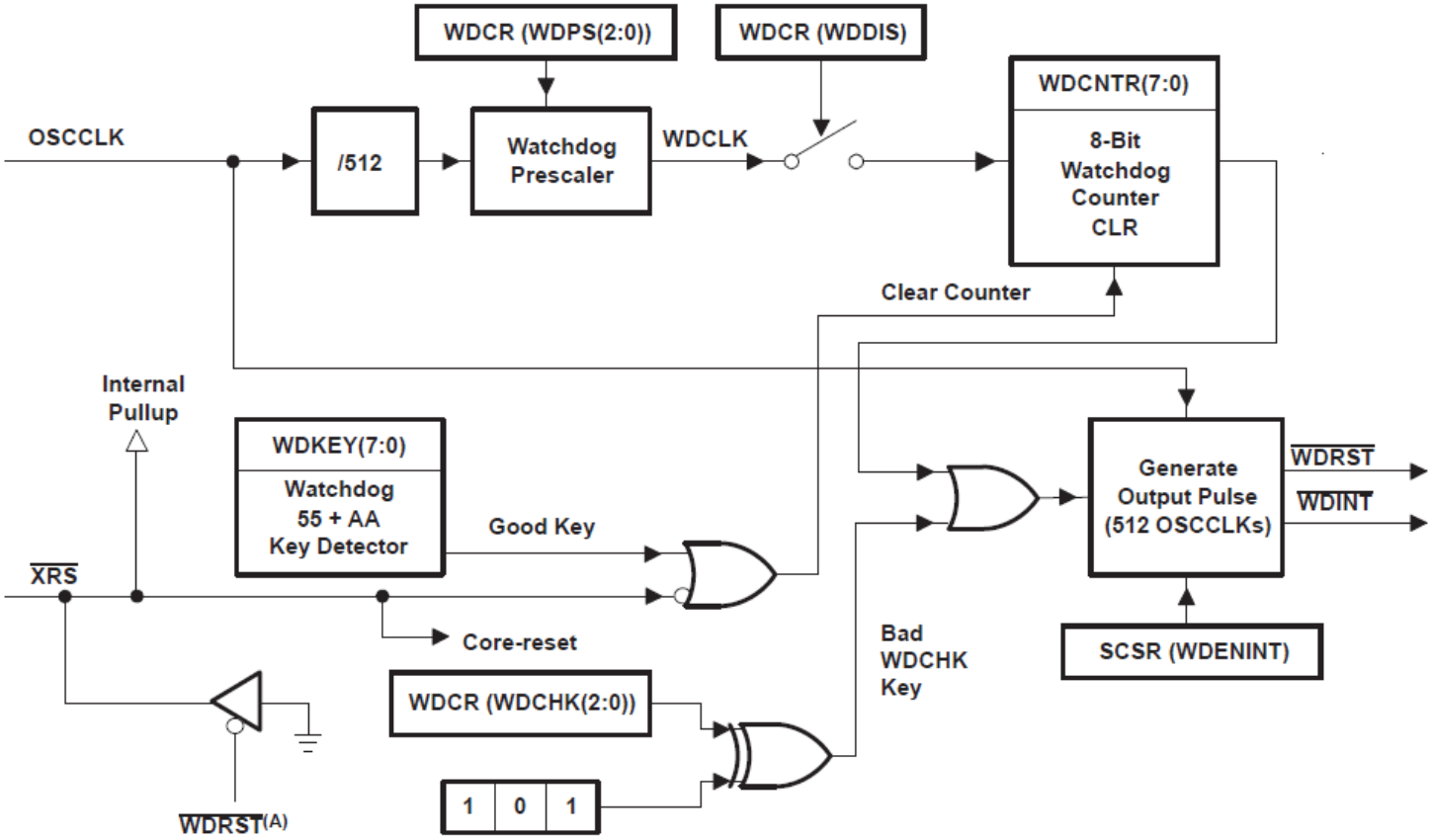
5、CPU定时器0/1/2

Watchdog Block

- 作用：确保在程序出错时自动复位系统。
- 运行模式：复位模式和中断模式。

1	WDENINT		Watchdog interrupt enable.
		0	The watchdog reset (WDRST) output signal is enabled and the watchdog interrupt (WDINT) output signal is disabled. This is the default state on reset (XRS). When the watchdog interrupt occurs the WDRST signal will stay low for 512 OSCCLK cycles. If the WDENINT bit is cleared while WDINT is low, a reset will immediately occur. The WDINTS bit can be read to determine the state of the WDINT signal.
		1	The WDRST output signal is disabled and the WDINT output signal is enabled. When the watchdog interrupt occurs, the WDINTsignal will stay low for 512 OSCCLK cycles. If the watchdog interrupt is used to wake the device from IDLE or STANDBY low power mode, use the WDINTS bit to make sure WDINT is not active before attempting to go back into IDLE or STANDBY mode.

Watchdog Block



A The WDRST and XRS signals are driven low for 512 OSCCLK cycles when a watchdog reset occurs. Likewise, if the watchdog interrupt is enabled, the WDINT signal will be driven low for 512 OSCCLK cycles when an interrupt occurs. Watchdog is not functional and cannot generate a reset when OSCCLK is not present.

Servicing The Watchdog Timer 喂狗

Step	Value Written to WDKEY	Result
1	0xAA	No action
2	0xAA	No action
3	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
4	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
5	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
6	0xAA	WDCNTR is reset.
7	0xAA	No action
8	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
9	0xAA	WDCNTR is reset.
10	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
11	0x32	Improper value written to WDKEY. No action, WDCNTR no longer enabled to be reset by next 0xAA.
12	0xAA	No action due to previous invalid value.
13	0x55	WDCNTR is enabled to be reset if next value is 0xAA.
14	0xAA	WDCNTR is reset.

第四讲：系统时钟

1、OSC和PLL模块

2、外设时钟信号

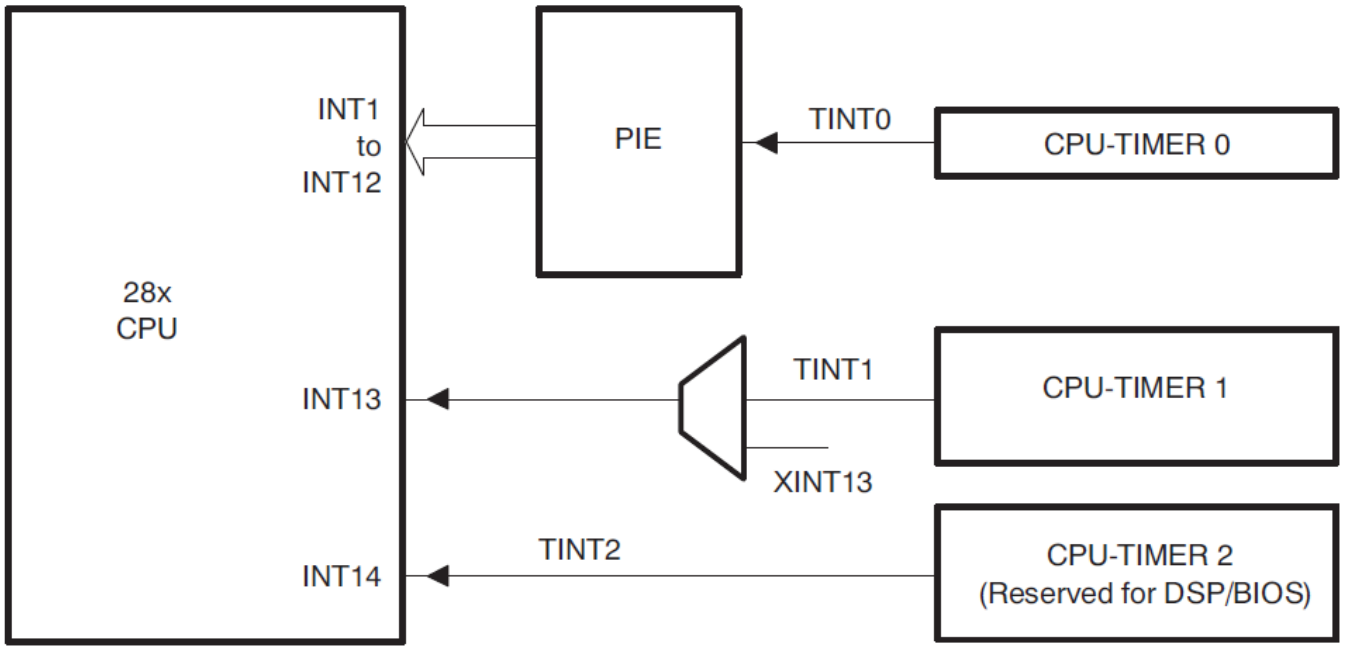
3、低功耗模式

4、Watchdog看门狗模块

5、CPU定时器0/1/2

Timer0/1/2中断信号连接方式

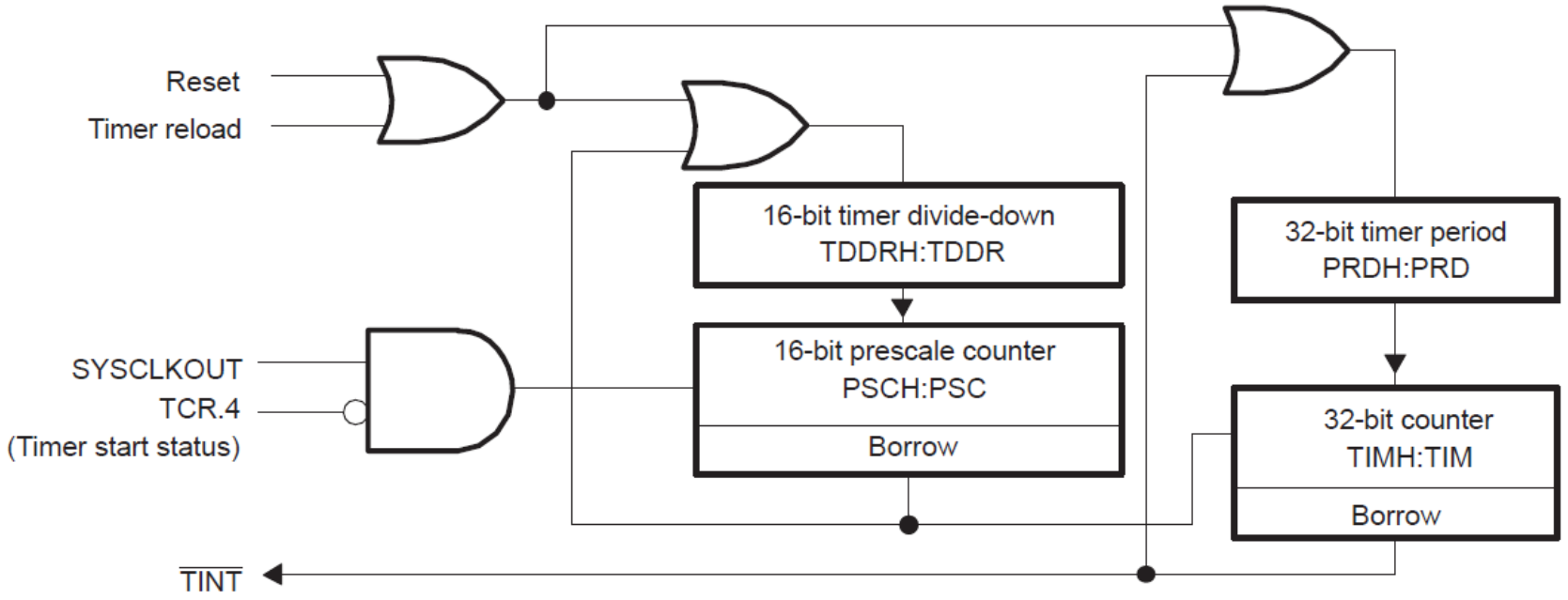
Timer0/1/2都可以为CPU产生中断信号



A The timer registers are connected to the Memory Bus of the 28x processor.

B The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

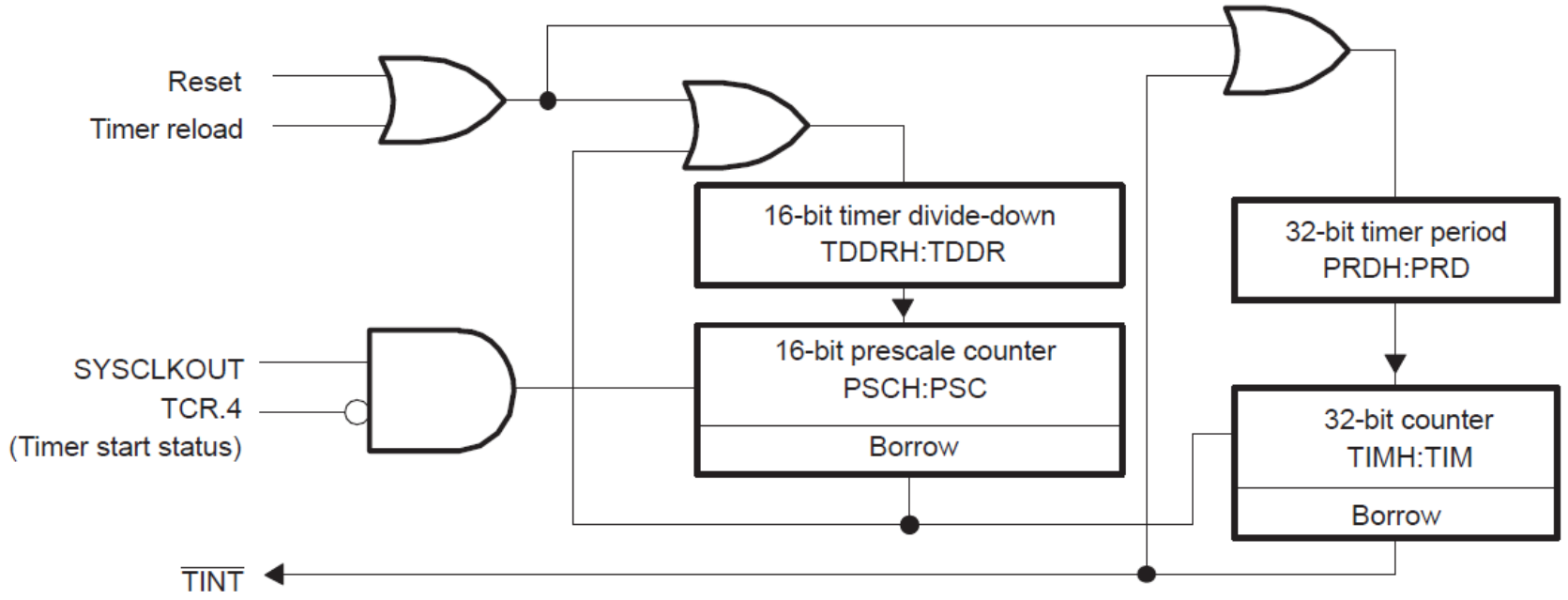
Timer0/1/2工作原理



Bits	Field	Description
15-0	TIM	CPU-Timer Counter Registers (TIMH:TIM): The TIM register holds the low 16 bits of the current 32-bit count of the timer. The TIMH register holds the high 16 bits of the current 32-bit count of the timer. The TIMH:TIM decrements by one every (TDDRH:TDDR+1) clock cycles, where TDDRH:TDDR is the timer prescale divide-down value. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers. The timer interrupt (TINT) signal is generated.

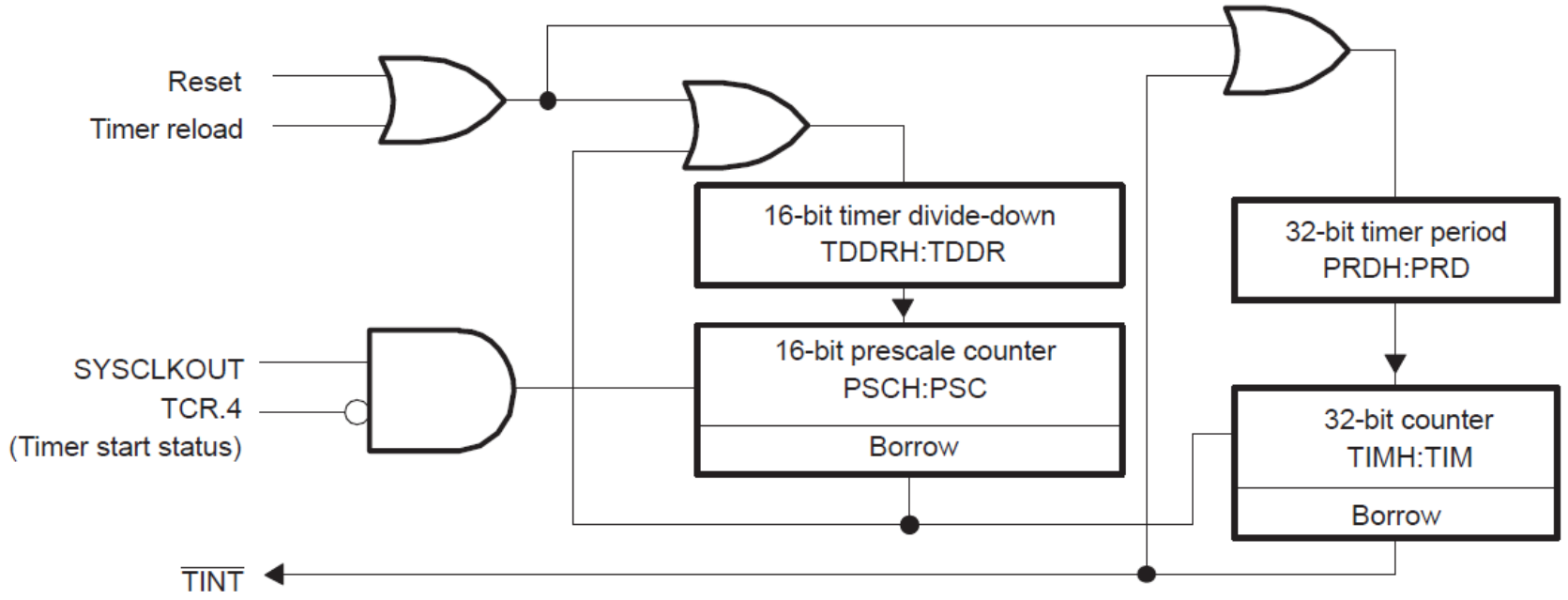
Bits	Field	Description
15-0	PRD	CPU-Timer Period Registers (PRDH:PRD): The PRD register holds the low 16 bits of the 32-bit period. The PRDH register holds the high 16 bits of the 32-bit period. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers, at the start of the next timer input clock cycle (the output of the prescaler). The PRDH:PRD contents are also loaded into the TIMH:TIM when you set the timer reload bit (TRB) in the Timer Control Register (TCR).

Timer0/1/2工作原理



Bits	Field	Description
15-8	PSC	CPU-Timer Prescale Counter. These bits hold the current prescale count for the timer. For every timer clock source cycle that the PSCH:PSC value is greater than 0, the PSCH:PSC decrements by one. One timer clock (output of the timer prescaler) cycle after the PSCH:PSC reaches 0, the PSCH:PSC is loaded with the contents of the TDDRH:TDDR, and the timer counter register (TIMH:TIM) decrements by one. The PSCH:PSC is also reloaded whenever the timer reload bit (TRB) is set by software. The PSCH:PSC can be checked by reading the register, but it cannot be set directly. It must get its value from the timer divide-down register (TDDRH:TDDR). At reset, the PSCH:PSC is set to 0.
7-0	TDDR	CPU-Timer Divide-Down. Every (TDDRH:TDDR + 1) timer clock source cycles, the timer counter register (TIMH:TIM) decrements by one. At reset, the TDDRH:TDDR bits are cleared to 0. To increase the overall timer count by an integer factor, write this factor minus one to the TDDRH:TDDR bits. When the prescaler counter (PSCH:PSC) value is 0, one timer clock source cycle later, the contents of the TDDRH:TDDR reload the PSCH:PSC, and the TIMH:TIM decrements by one. TDDRH:TDDR also reloads the PSCH:PSC whenever the timer reload bit (TRB) is set by software.

Timer0/1/2工作原理



4	TSS		CPU-Timer stop status bit. TSS is a 1-bit flag that stops or starts the CPU-timer.
		0	Reads of 0 indicate the CPU-timer is running. To start or restart the CPU-timer, set TSS to 0. At reset, TSS is cleared to 0 and the CPU-timer immediately starts.
		1	Reads of 1 indicate that the CPU-timer is stopped. To stop the CPU-timer, set TSS to 1.


谢谢