第五讲　系统中断

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第五讲：系统中断

1、中断概述

2、外设中断扩展模块PIE

3、中断向量列表

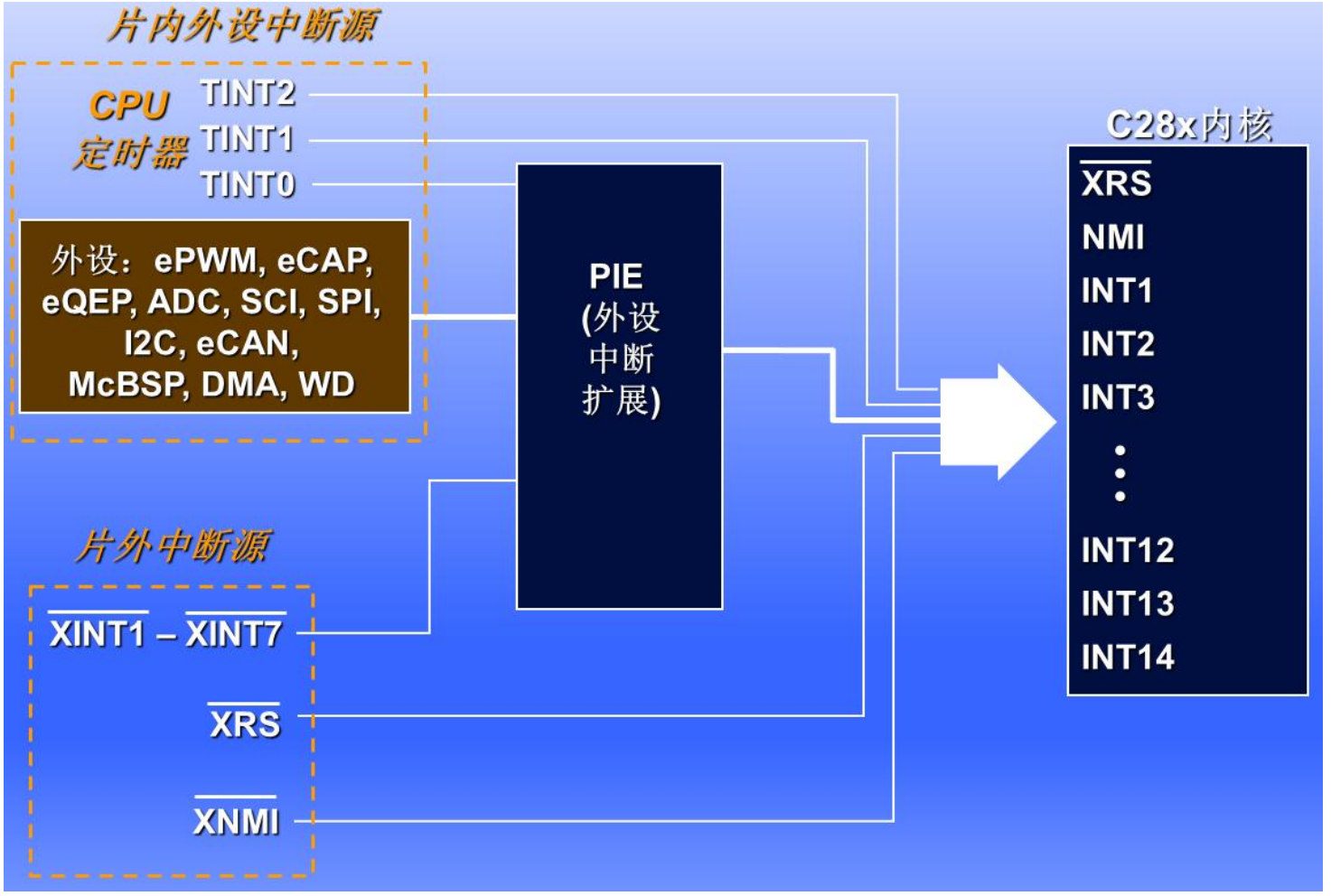
中断概述

◆CPU进行正常程序处理的时候，有时会被要求接收更高级别指令或实时性要求更高的任务，不得不中断当前的程序处理，而去响应后者，即进入新的中断服务程序（interrupt service routine）。

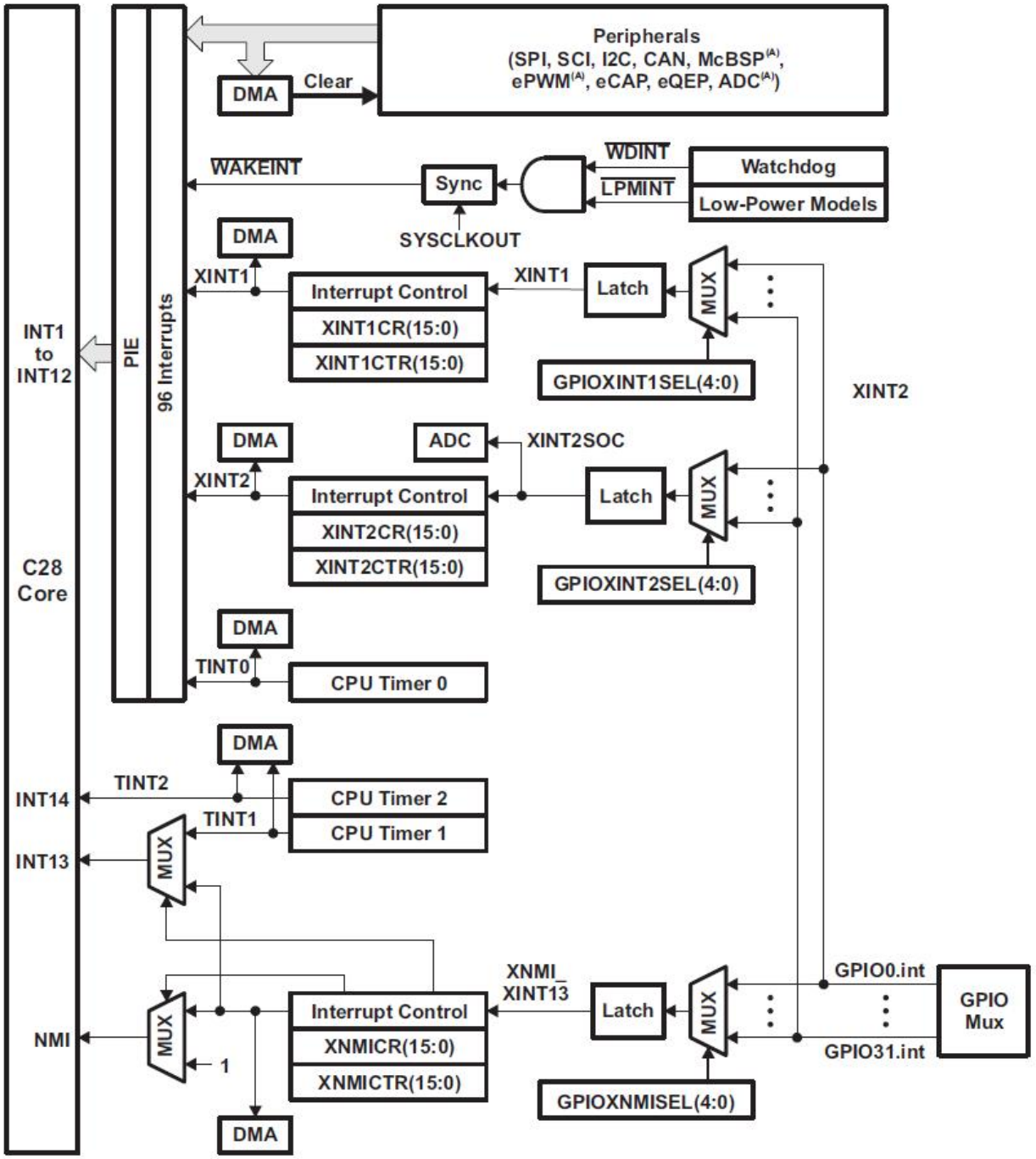
◆F28335有很多的外设，这些外设与相关资源都有可能发布新的任务让内核来判断与处理，也就是F28335的可能中断源有很多。F28335的中断源可分为片内外设中断源，如PWM、CAP、QEP、定时器等，片外中断源，如外部中断输入引脚XINT1、XINT2引入的外部中断源。这些中断源将中断请求信号传递给内核就肯定需要中断线，F28335的中断线是有限的。

中断源

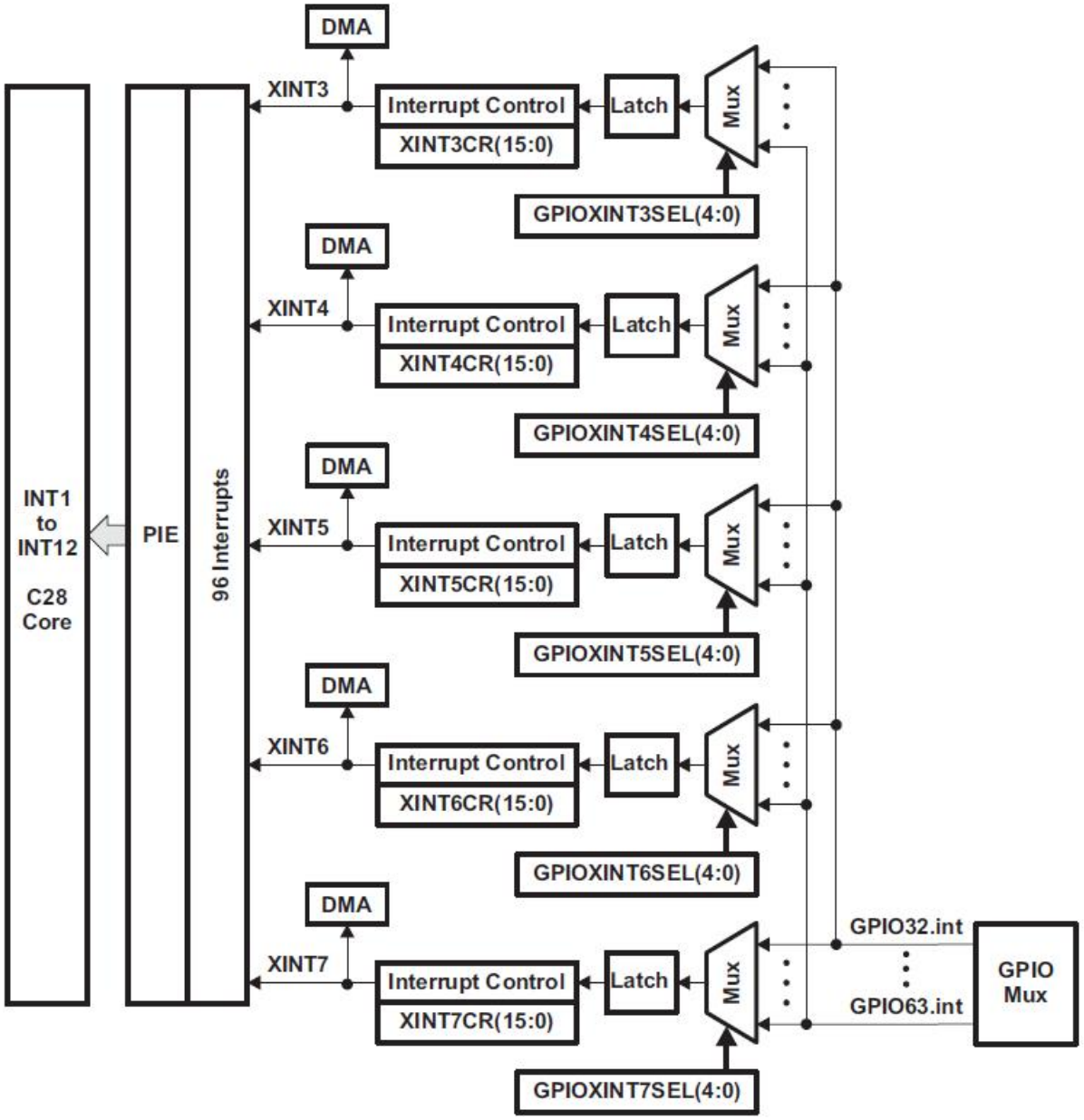
◆F28335内部有16个中断线，其中包括2个不可屏蔽中断（RESET和NMI）与14个可屏蔽中断。



中断源

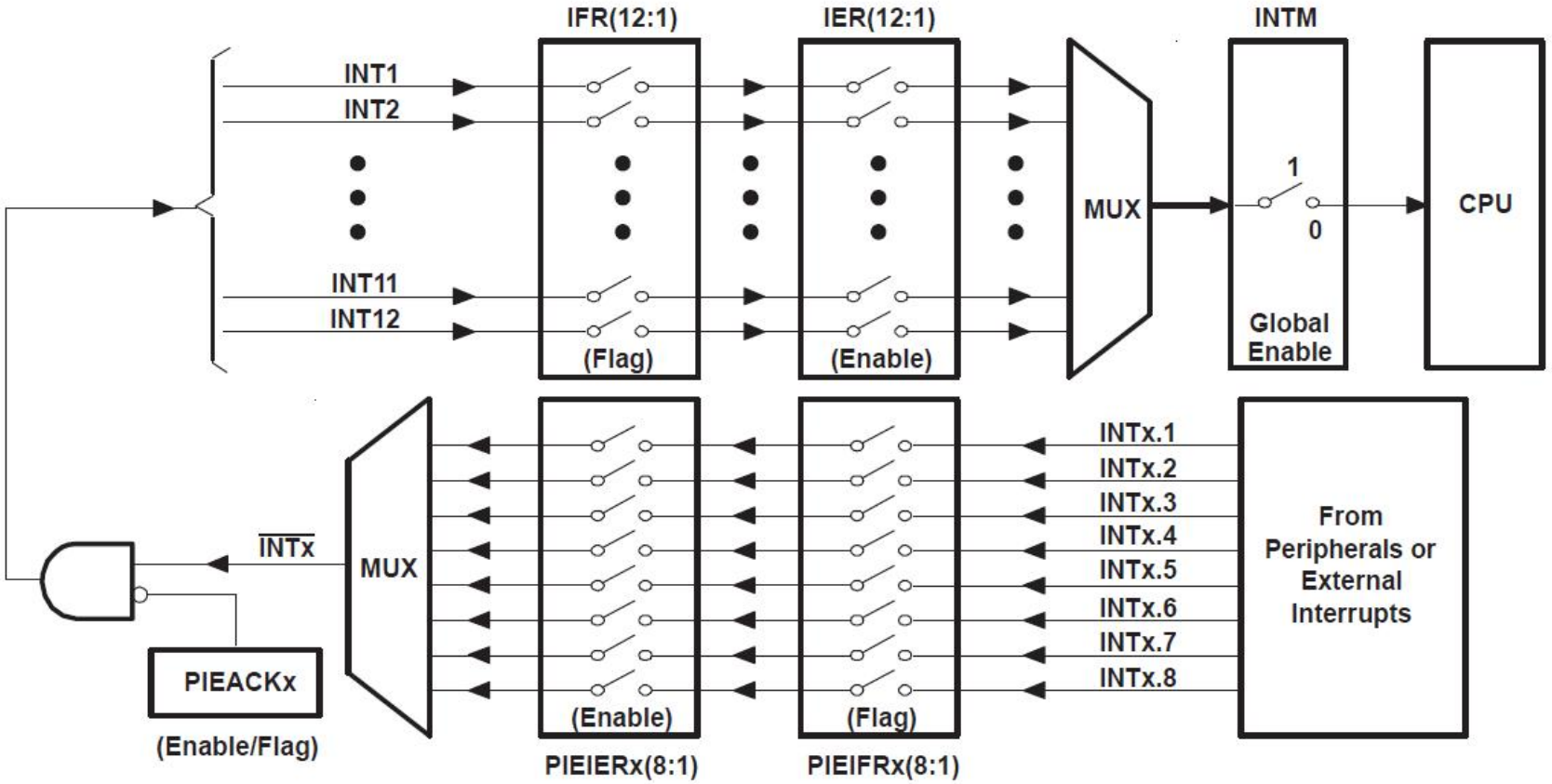

Peripherals
(SPI, SCI, I2C, CAN, McBSP(A),
ePWM(A), eCAP, eQEP, ADC(A))
DMA
Clear
WDINT
LPMINT
Watchdog
Low-Power Models
WAKEINT
Sync
SYSCLKOUT
DMA
XINT1
Interrupt Control
XINT1CR(15:0)
XINT1CTR(15:0)
XINT1
Latch
MUX
GPIOXINT1SEL(4:0)
XINT2
INT1
to
INT12
PIE
96 Interrupts
DMA
ADC
XINT2SOC
XINT2
Interrupt Control
XINT2CR(15:0)
XINT2CTR(15:0)
Latch
MUX
GPIOXINT2SEL(4:0)
C28
Core
DMA
TINT0
CPU Timer 0
DMA
TINT2
INT14
CPU Timer 2
TINT1
CPU Timer 1
INT13
MUX
XNMI_
XINT13
GPIO0.int
Interrupt Control
XNMICR(15:0)
XNMICTR(15:0)
Latch
MUX
GPIO
Mux
NMI
MUX
1
GPIO31.int
GPIOXNMISEL(4:0)
DMA

中断源


DMA
XINT3
Interrupt Control
XINT3CR(15:0)
Latch
Mux
GPIOXINT3SEL(4:0)
DMA
XINT4
Interrupt Control
XINT4CR(15:0)
Latch
Mux
GPIOXINT4SEL(4:0)
DMA
XINT5
Interrupt Control
XINT5CR(15:0)
Latch
Mux
GPIOXINT5SEL(4:0)
DMA
XINT6
Interrupt Control
XINT6CR(15:0)
Latch
Mux
GPIOXINT6SEL(4:0)
DMA
XINT7
Interrupt Control
XINT7CR(15:0)
Latch
Mux
GPIOXINT7SEL(4:0)
INT1
to
INT12
C28
Core
PIE
96 Interrupts
GPIO32.int
GPIO63.int
GPIO
Mux

中断机制

◆F28335的中断采用的是三级中断机制，分别为外设级中断、PIE级中断和CPU级中断。在有限中断线的情况下，只能安排中断线进行复用。



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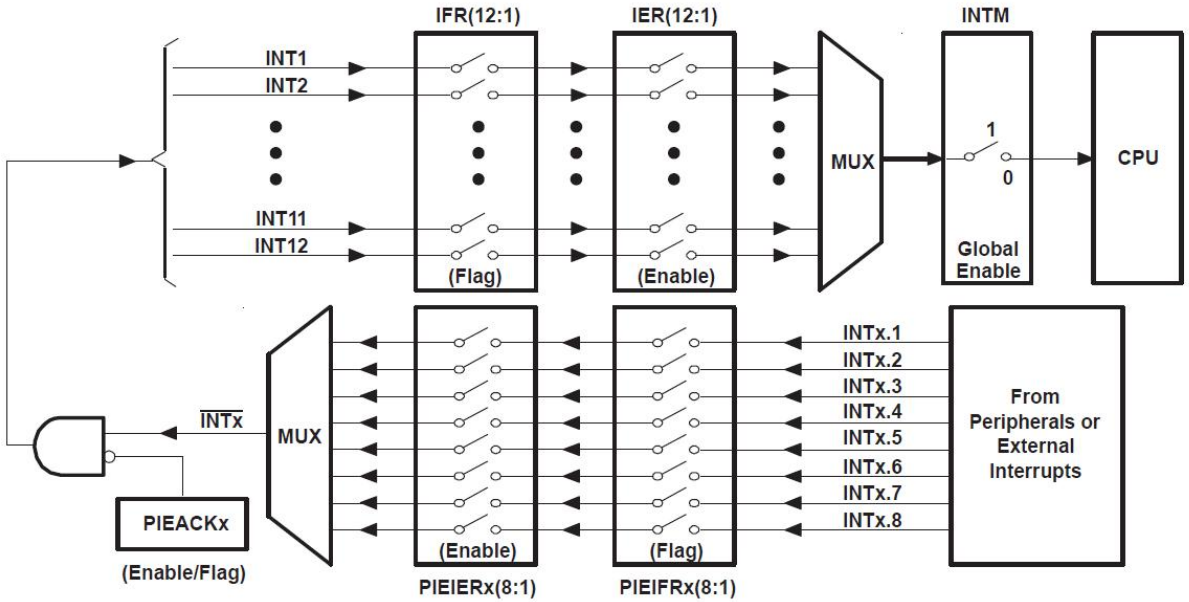
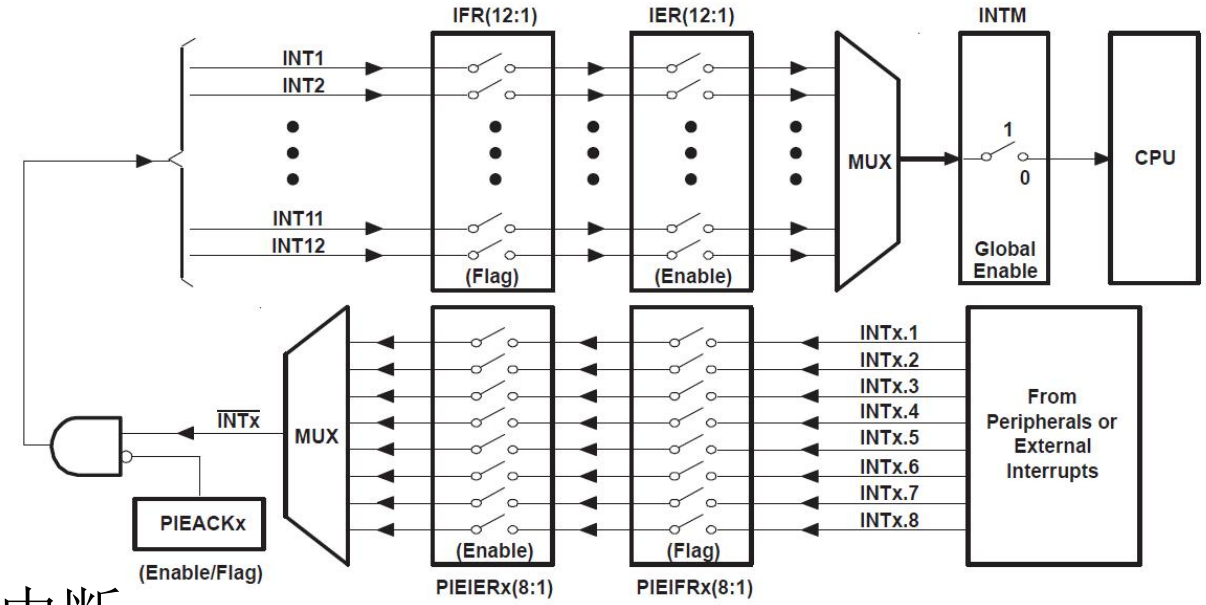
使用PIE模块处理中断



1. 外设级中断

当外设有中断事件发生时，该外设相关寄存器中的中断标志位（IF）将置1，如果该外设相关寄存器中的中断使能位（IE）也为1，那么此次中断事件将向PIE发出中断请求信号，如果其中断使能位为0，中断标志位IF将保持为1，直到被软件清零。如果之后IE被置1，此时IF如果仍为1，也将会向PIE发出中断请求信号。

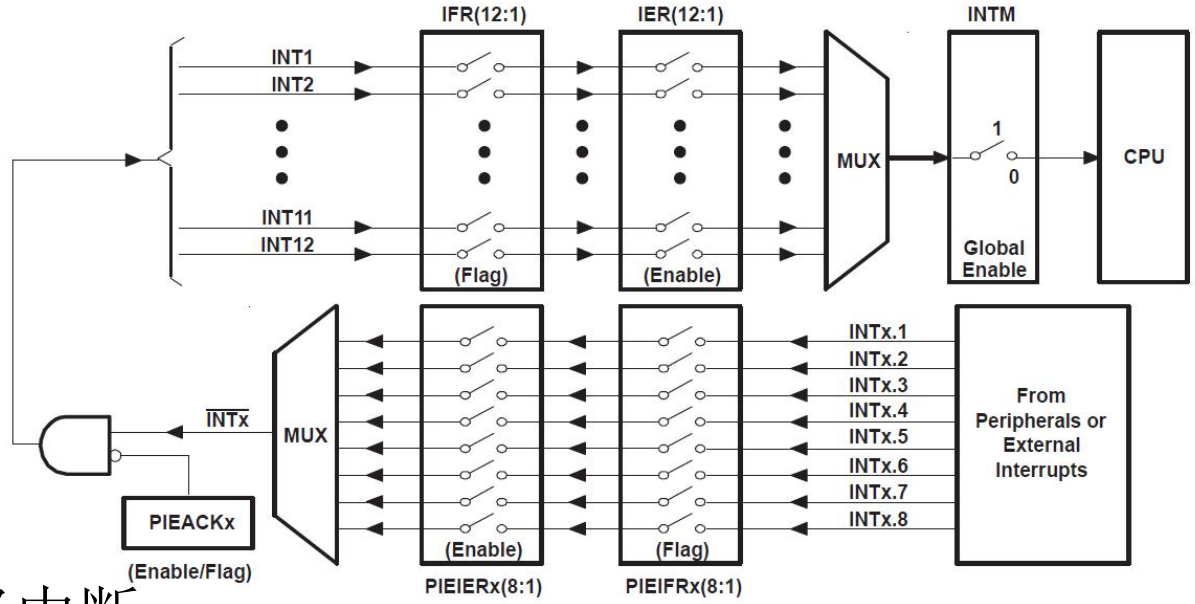
使用PIE模块处理中断



2. PIE级中断

一旦外设或外部引脚向PIE模块发出中断请求信号，相应的中断标志位PIEIFx.y置1。如果相应的中断使能位PIEIEx.y=1，PIE模块将检测该组的确认信号PIEACKx以判断CPU是否可以接收该组的中断请求信号，如果PIEACKx=0，PIE向CPU的INTx口发出中断请求信号，如果PIEACKx=1，PIE将进入等待状态，直到PIEACKx被清零后才向CPU发出中断请求信号。

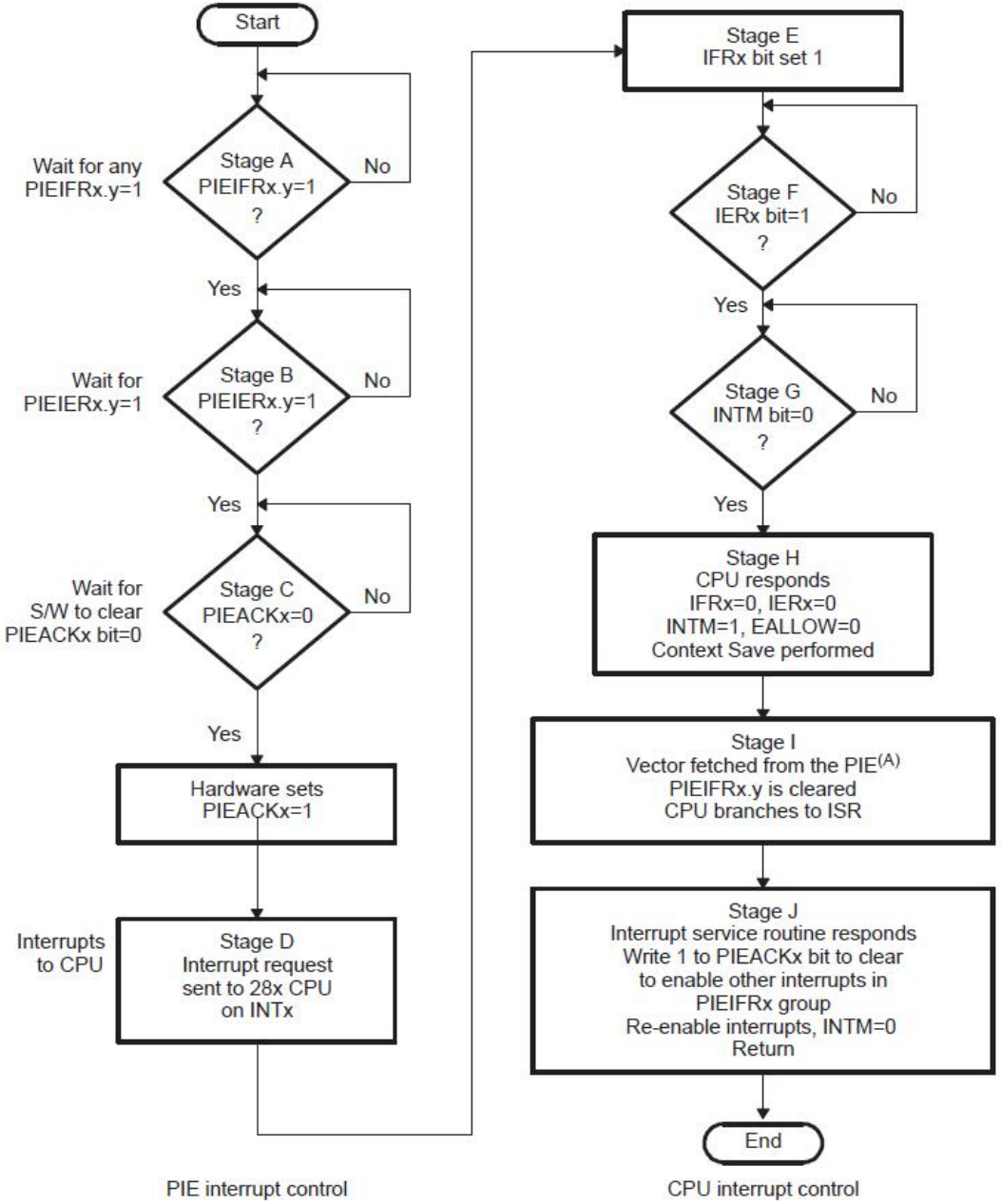
使用PIE模块处理中断



3. CPU级中断

一旦中断请求信号送到CPU级，与INTx对应的CPU中断标志寄存器IFR中的相应位将置1，如果中断使能寄存器IER中的相应位为1，且全局使能位INTM=0或DBGIER=1（与使用的中断处理进程有关），CPU响应中断请求：首先自动将IERx、IFRx、EALLOW清零，将INTM置1，然后从PIE中断向量列表中读取中断服务函数的地址，转入中断服务函数地址处开始执行，执行完毕后返回。

PIE/CPU中断响应流程



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PIE多路复用外设中断向量表

INTX	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
1	WAKE	TIMER0	ADC	XINT2	XINT1	保留	SEQ2	SEQ1
2	保留	保留	EPWM6_TZINT	EPWM5_TZINT	EPWM4_TZINT	EPWM3_TZINT	EPWM2_TZINT	EPWM1_TZINT
3	保留	保留	EPWM6_INT	EPWM5_INT	EPWM4_INT	EPWM3_INT	EPWM2_INT	EPWM1_INT
4	保留	保留	ECAP6_INT	ECAP5_INT	ECAP4_INT	ECAP3_INT	ECAP2_INT	ECAP1_INT
5	保留	保留	保留	保留	保留	保留	EQEP1_INT	EQEP1_INT
6	保留	保留	MXINTB	MRINTB	MXINTA	MRINTA	SPITXINTA	SPIRXINTA
7	保留	保留	DINTCH6	DINTCH5	DINTCH4	DINTCH3	DINTCH2	DINTCH1
8	保留	保留	SCITXINTC	SCIRXINTC	保留	保留	I2CINT2A	I2CINT1A
9	ECAN1INTB	ECAN01NTB	ECAN1INTA	ECAN01NTA	SCITXINTB	SCIRXINT	SCITXINTA	SCIRXINTA
10	保留	保留	保留	保留	保留	保留	保留	保留
11	保留	保留	保留	保留	保留	保留	保留	保留
12	LUF	LVF	保留	XINT7	XINT6	XINT5	XINT4	XINT3

PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]	CPU Priority	PIE Group Priority
Reset	0	0x0000 0D00	2	Reset is always fetched from location 0x003F FFC0 in Boot ROM.	1 (highest)	-
INT1	1	0x0000 0D02	2	Not used. See PIE Group 1	5	-
INT2	2	0x0000 0D04	2	Not used. See PIE Group 2	6	-
INT3	3	0x0000 0D06	2	Not used. See PIE Group 3	7	-
INT4	4	0x0000 0D08	2	Not used. See PIE Group 4	8	-
INT5	5	0x0000 0D0A	2	Not used. See PIE Group 5	9	-
INT6	6	0x0000 0D0C	2	Not used. See PIE Group 6	10	-
INT7	7	0x0000 0D0E	2	Not used. See PIE Group 7	11	-
INT8	8	0x0000 0D10	2	Not used. See PIE Group 8	12	-
INT9	9	0x0000 0D12	2	Not used. See PIE Group 9	13	-
INT10	10	0x0000 0D14	2	Not used. See PIE Group 10	14	-
INT11	11	0x0000 0D16	2	Not used. See PIE Group 11	15	-
INT12	12	0x0000 0D18	2	Not used. See PIE Group 12	16	-
INT13	13	0x0000 0D1A	2	External Interrupt 13 (XINT13) or CPU-Timer1	17	-
INT14	14	0x0000 0D1C	2	CPU-Timer2 (for TI/RTOS use)	18	-
DATALOG	15	0x0000 0D1E	2	CPU Data Logging Interrupt	19 (lowest)	-
RTOSINT	16	0x0000 0D20	2	CPU Real-Time OS Interrupt	4	-
EMUINT	17	0x0000 0D22	2	CPU Emulation Interrupt	2	-
NMI	18	0x0000 0D24	2	External Non-Maskable Interrupt	3	-
ILLEGAL	19	0x0000 0D26	2	Illegal Operation	-	-
USER1	20	0x0000 0D28	2	User-Defined Trap	-	-
USER2	21	0x0000 0D2A	2	User Defined Trap	-	-
USER3	22	0x0000 0D2C	2	User Defined Trap	-	-
USER4	23	0x0000 0D2E	2	User Defined Trap	-	-
USER5	24	0x0000 0D30	2	User Defined Trap	-	-
USER6	25	0x0000 0D32	2	User Defined Trap	-	-
USER7	26	0x0000 0D34	2	User Defined Trap	-	-
USER8	27	0x0000 0D36	2	User Defined Trap	-	-
USER9	28	0x0000 0D38	2	User Defined Trap	-	-
USER10	29	0x0000 0D3A	2	User Defined Trap	-	-
USER11	30	0x0000 0D3C	2	User Defined Trap	-	-
USER12	31	0x0000 0D3E	2	User Defined Trap	-	-

PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 1 Vectors - MUXed into CPU INT1							
INT1.1	32	0x0000 0D40	2	SEQ1INT	(ADC)	5	1 (highest)
INT1.2	33	0x0000 0D42	2	SEQ2INT	(ADC)	5	2
INT1.3	34	0x0000 0D44	2	Reserved		5	3
INT1.4	35	0x0000 0D46	2	XINT1		5	4
INT1.5	36	0x0000 0D48	2	XINT2		5	5
INT1.6	37	0x0000 0D4A	2	ADCINT	(ADC)	5	6
INT1.7	38	0x0000 0D4C	2	TINT0	(CPU-Timer0)	5	7
INT1.8	39	0x0000 0D4E	2	WAKEINT	(LPM/WD)	5	8 (lowest)
PIE Group 2 Vectors - MUXed into CPU INT2							
INT2.1	40	0x0000 0D50	2	EPWM1_TZINT	(EPWM1)	6	1 (highest)
INT2.2	41	0x0000 0D52	2	EPWM2_TZINT	(EPWM2)	6	2
INT2.3	42	0x0000 0D54	2	EPWM3_TZINT	(EPWM3)	6	3
INT2.4	43	0x0000 0D56	2	EPWM4_TZINT	(EPWM4)	6	4
INT2.5	44	0x0000 0D58	2	EPWM5_TZINT	(EPWM5)	6	5
INT2.6	45	0x0000 0D5A	2	EPWM6_TZINT	(EPWM6)	6	6
INT2.7	46	0x0000 0D5C	2	Reserved		6	7
INT2.8	47	0x0000 0D5E	2			6	8 (lowest)

PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 3 Vectors - MUXed into CPU INT3							
INT3.1	48	0x0000 0D60	2	EPWM1_INT	(EPWM1)	7	1 (highest)
INT3.2	49	0x0000 0D62	2	EPWM2_INT	(EPWM2)	7	2
INT3.3	50	0x0000 0D64	2	EPWM3_INT	(EPWM3)	7	3
INT3.4	51	0x0000 0D66	2	EPWM4_INT	(EPWM4)	7	4
INT3.5	52	0x0000 0D68	2	EPWM5_INT	(EPWM5)	7	5
INT3.6	53	0x0000 0D6A	2	EPWM6_INT	(EPWM6)	7	6
INT3.7	54	0x0000 0D6C	2	Reserved		7	7
INT3.8	55	0x0000 0D6E	2	Reserved		7	8 (lowest)
PIE Group 4 Vectors - MUXed into CPU INT4							
INT4.1	56	0x0000 0D70	2	ECAP1_INT	(ECAP1)	8	1 (highest)
INT4.2	57	0x0000 0D72	2	ECAP2_INT	(ECAP2)	8	2
INT4.3	58	0x0000 0D74	2	ECAP3_INT	(ECAP3)	8	3
INT4.4	59	0x0000 0D76	2	ECAP4_INT	(ECAP4)	8	4
INT4.5	60	0x0000 0D78	2	ECAP5_INT	(ECAP5)	8	5
INT4.6	61	0x0000 0D7A	2	ECAP6_INT	(ECAP6)	8	6
INT4.7	62	0x0000 0D7C	2	Reserved		8	7
INT4.8	63	0x0000 0D7E	2	Reserved		8	8 (lowest)

PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 5 Vectors - MUXed into CPU INT5							
INT5.1	64	0x0000 0D80	2	EQEP1_INT	(EQEP1)	9	1 (highest)
INT5.2	65	0x0000 0D82	2	EQEP2_INT	(EQEP2)	9	2
INT5.3	66	0x0000 0D84	2	Reserved		9	3
INT5.4	67	0x0000 0D86	2	Reserved		9	4
INT5.5	68	0x0000 0D88	2	Reserved		9	5
INT5.6	69	0x0000 0D8A	2	Reserved		9	6
INT5.7	70	0x0000 0D8C	2	Reserved		9	7
INT5.8	71	0x0000 0D8E	2	Reserved		9	8 (lowest)
PIE Group 6 Vectors - MUXed into CPU INT6							
INT6.1	72	0x0000 0D90	2	SPIRXINTA	(SPI-A)	10	1 (highest)
INT6.2	73	0x0000 0D92	2	SPITXINTA	(SPI-A)	10	2
INT6.3	74	0x0000 0D94	2	MRINTB	(McBSP-B)	10	3
INT6.4	75	0x0000 0D96	2	MXINTB	(McBSP-B)(SPI-B)	10	4
INT6.5	76	0x0000 0D98	2	MRINTA	(McBSP-A)	10	5
INT6.6	77	0x0000 0D9A	2	MXINTA	(McBSP-A)	10	6
INT6.7	78	0x0000 0D9C	2	Reserved		10	7
INT6.8	79	0x0000 0D9E	2	Reserved		10	8 (lowest)

PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 7 Vectors - MUXed into CPU INT7							
INT7.1	80	0x0000 0DA0	2	DINTCH1	DMA Channel 1	11	1 (highest)
INT7.2	81	0x0000 0DA2	2	DINTCH2	DMA Channel 2	11	2
INT7.3	82	0x0000 0DA4	2	DINTCH3	DMA Channel 3	11	3
INT7.4	83	0x0000 0DA6	2	DINTCH4	DMA Channel 4	11	4
INT7.5	84	0x0000 0DA8	2	DINTCH5	DMA Channel 5	11	5
INT7.6	85	0x0000 0DAA	2	DINTCH6	DMA Channel 6	11	6
INT7.7	86	0x0000 0DAC	2	Reserved	-	11	7
INT7.8	87	0x0000 0DAE	2	Reserved	-	11	8 (lowest)
PIE Group 8 Vectors - MUXed into CPU INT8							
INT8.1	88	0x0000 0DB0	2	I2CINT1A	(I2C-A)	12	1 (highest)
INT8.2	89	0x0000 0DB2	2	I2CINT2A	(I2C-A)	12	2
INT8.3	90	0x0000 0DB4	2	Reserved	-	12	3
INT8.4	91	0x0000 0DB6	2	Reserved	-	12	4
INT8.5	92	0x0000 0DB8	2	SCIRXINTC	(SCI-C)	12	5
INT8.6	93	0x0000 0DBA	2	SCITXINTC	(SCI-C)	12	6
INT8.7	94	0x0000 0DBC	2	Reserved	-	12	7
INT8.8	95	0x0000 0DBE	2	Reserved	-	12	8 (lowest)

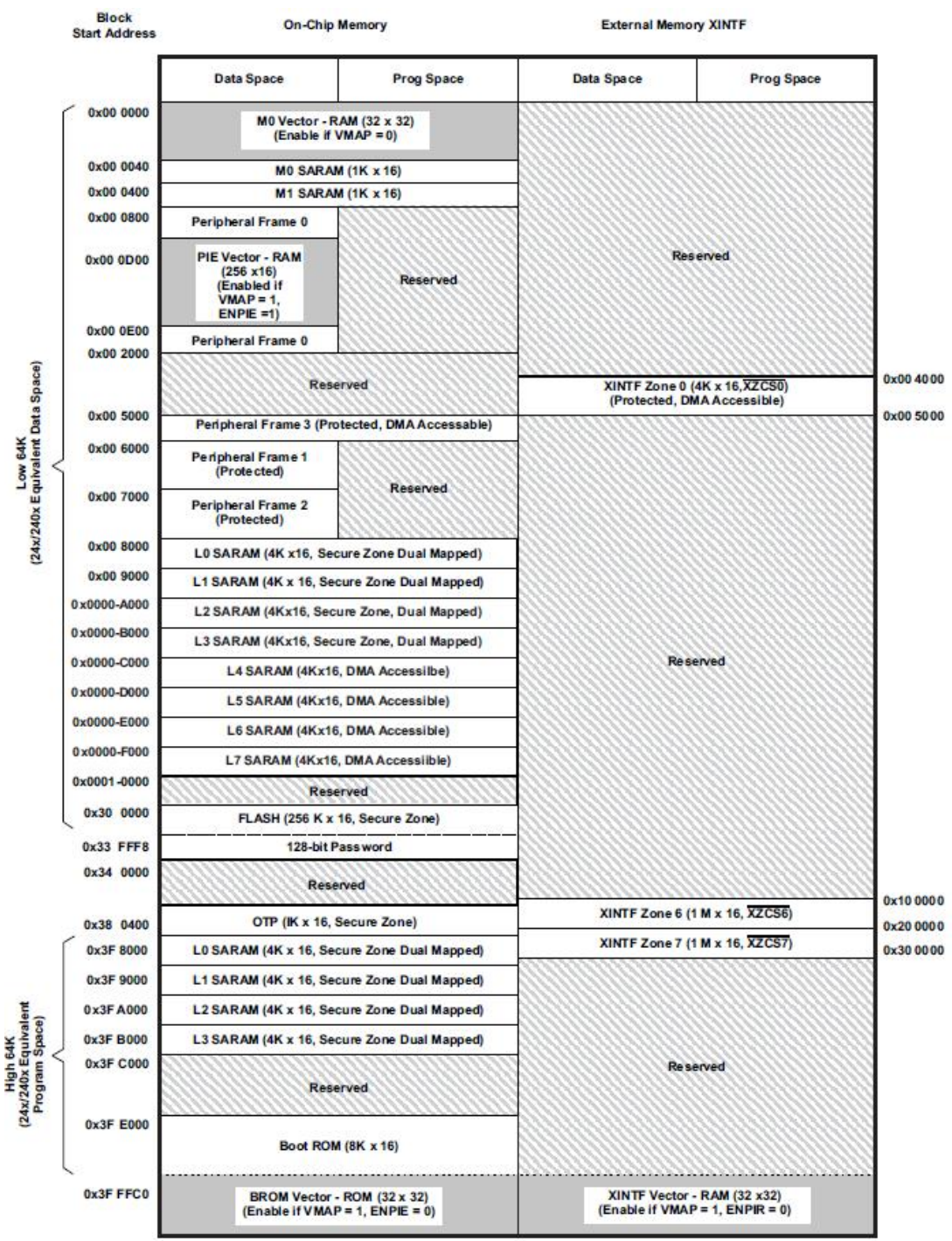
PIE中断向量表

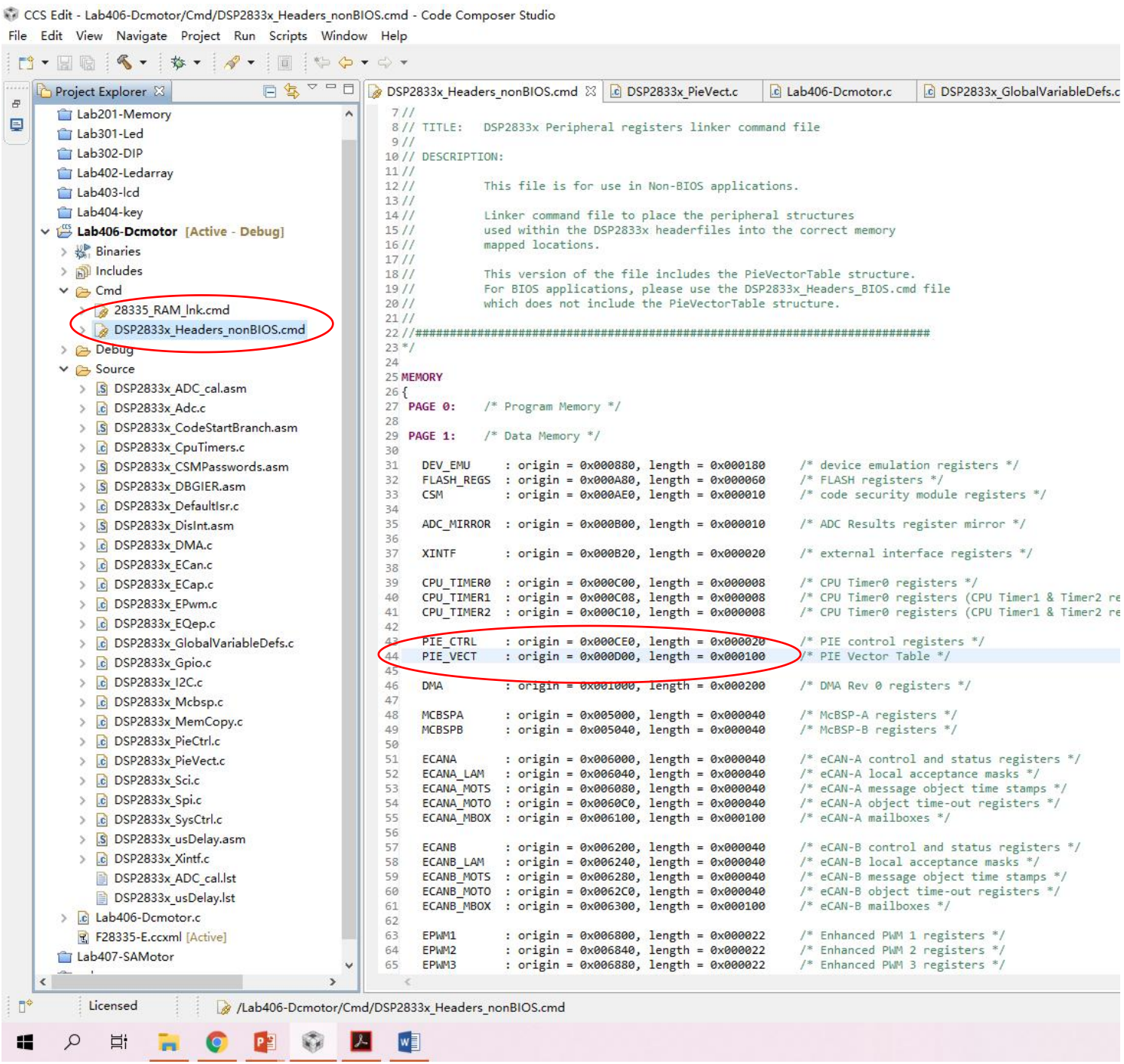
Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 9 Vectors - MUXed into CPU INT9							
INT9.1	96	0x0000 0DC0	2	SCIRXINTA	(SCI-A)	13	1 (highest)
INT9.2	97	0x0000 0DC2	2	SCITXINTA	(SCI-A)	13	2
INT9.3	98	0x0000 0DC4	2	SCIRXINTB	(SCI-B)	13	3
INT9.4	99	0x0000 0DC6	2	SCITXINTB	(SCI-B)	13	4
INT9.5	100	0x0000 0DC8	2	ECAN0INTA	(eCAN-A)	13	5
INT9.6	101	0x0000 0DCA	2	ECAN1INTA	(eCAN-A)	13	6
INT9.7	102	0x0000 0DCC	2	ECAN0INTB	(eCAN-B)	13	7
INT9.8	103	0x0000 0DCE	2	ECAN1INTB	(eCAN-B)	13	8 (lowest)
PIE Group 10 Vectors - MUXed into CPU INT10							
INT10.1	104	0x0000 0DD0	2	Reserved	-	14	1 (highest)
INT10.2	105	0x0000 0DD2	2	Reserved		14	2
INT10.3	106	0x0000 0DD4	2	Reserved		14	3
INT10.4	107	0x0000 0DD6	2	Reserved		14	4
INT10.5	108	0x0000 0DD8	2	Reserved		14	5
INT10.6	109	0x0000 0DDA	2	Reserved		14	6
INT10.7	110	0x0000 0DDC	2	Reserved		14	7
INT10.8	111	0x0000 0DDE	2	Reserved		14	8 (lowest)

PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 11 Vectors - MUXed into CPU INT11							
INT11.1	112	0x0000 0DE0	2	Reserved		15	1 (highest)
INT11.2	113	0x0000 0DE2	2	Reserved		15	2
INT11.3	114	0x0000 0DE4	2	Reserved		15	3
INT11.4	115	0x0000 0DE6	2	Reserved		15	4
INT11.5	116	0x0000 0DE8	2	Reserved		15	5
INT11.6	117	0x0000 0DEA	2	Reserved		15	6
INT11.7	118	0x0000 0DEC	2	Reserved		15	7
INT11.8	119	0x0000 0DEE	2	Reserved		15	8 (lowest)
PIE Group 12 Vectors - Muxed into CPU INT12							
INT12.1	120	0x0000 0DF0	2	XINT3		16	1 (highest)
INT12.2	121	0x0000 0DF2	2	XINT4		16	2
INT12.3	122	0x0000 0DF4	2	XINT5		16	3
INT12.4	123	0x0000 0DF6	2	XINT6		16	4
INT12.5	124	0x0000 0DF8	2	XINT7		16	5
INT12.6	125	0x0000 0DFA	2	Reserved		16	6
INT12.7	126	0x0000 0DFC	2	LVF	FPU	16	7
INT12.8	127	0x0000 0DFE	2	LUF	FPU	16	8 (lowest)

PIE中断向量地址


Block Start Address
On-Chip Memory
External Memory XINTF
Data Space
Prog Space
Data Space
Prog Space
0x00 0000
M0 Vector - RAM (32 x 32) (Enable if VMAP = 0)
0x00 0040
M0 SARAM (1K x 16)
0x00 0400
M1 SARAM (1K x 16)
0x00 0800
Peripheral Frame 0
0x00 0D00
PIE Vector - RAM (256 x16) (Enabled if VMAP = 1, ENPIE =1)
Reserved
Reserved
0x00 0E00
Peripheral Frame 0
0x00 2000
Reserved
XINTF Zone 0 (4K x 16, XZCS0) (Protected, DMA Accessible)
0x00 4000
0x00 5000
Peripheral Frame 3 (Protected, DMA Accessable)
0x00 5000
0x00 6000
Peripheral Frame 1 (Protected)
Reserved
0x00 7000
Peripheral Frame 2 (Protected)
Low 64K (24x/240x Equivalent Data Space)
0x00 8000
L0 SARAM (4K x16, Secure Zone Dual Mapped)
0x00 9000
L1 SARAM (4K x 16, Secure Zone Dual Mapped)
0x0000-A000
L2 SARAM (4Kx16, Secure Zone, Dual Mapped)
0x0000-B000
L3 SARAM (4Kx16, Secure Zone, Dual Mapped)
0x0000-C000
L4 SARAM (4Kx16, DMA Accessilbe)
0x0000-D000
L5 SARAM (4Kx16, DMA Accessible)
0x0000-E000
L6 SARAM (4Kx16, DMA Accessible)
0x0000-F000
L7 SARAM (4Kx16, DMA Accessible)
Reserved
0x0001-0000
0x30 0000
FLASH (256 K x 16, Secure Zone)
0x33 FFF8
128-bit Password
0x34 0000
Reserved
Reserved
0x10 0000
0x38 0400
OTP (IK x 16, Secure Zone)
XINTF Zone 6 (1 M x 16, XZCS6)
0x20 0000
0x3F 8000
L0 SARAM (4K x 16, Secure Zone Dual Mapped)
XINTF Zone 7 (1 M x 16, XZCS7)
0x30 0000
0x3F 9000
L1 SARAM (4K x 16, Secure Zone Dual Mapped)
0x3F A000
L2 SARAM (4K x 16, Secure Zone Dual Mapped)
0x3F B000
L3 SARAM (4K x 16, Secure Zone Dual Mapped)
High 64K (24x/240x Equivalent Program Space)
0x3F C000
Reserved
Reserved
0x3F E000
Boot ROM (8K x 16)
0x3F FFC0
BROM Vector - ROM (32 x 32) (Enable if VMAP = 1, ENPIE = 0)
XINTF Vector - RAM (32 x32) (Enable if VMAP = 1, ENPIR = 0)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DSP2833x_Gpio.c
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DSP2833x_Headers_nonBIOS.cmd
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DSP2833x_GlobalVariableDefs.c
// TITLE: DSP2833x Peripheral registers linker command file
// DESCRIPTION:
// This file is for use in Non-BIOS applications.
// Linker command file to place the peripheral structures
// used within the DSP2833x headerfiles into the correct memory
// mapped locations.
// This version of the file includes the PieVectorTable structure.
// For BIOS applications, please use the DSP2833x_Headers_BIOS.cmd file
// which does not include the PieVectorTable structure.
MEMORY
{
PAGE 0: /* Program Memory */
PAGE 1: /* Data Memory */
DEV_EMU : origin = 0x000880, length = 0x000180 /* device emulation registers */
FLASH_REGS : origin = 0x000A80, length = 0x000060 /* FLASH registers */
CSM : origin = 0x000AE0, length = 0x000010 /* code security module registers */
ADC_MIRROR : origin = 0x000B00, length = 0x000010 /* ADC Results register mirror */
XINTF : origin = 0x000B20, length = 0x000020 /* external interface registers */
CPU_TIMER0 : origin = 0x000C00, length = 0x000008 /* CPU Timer0 registers */
CPU_TIMER1 : origin = 0x000C08, length = 0x000008 /* CPU Timer0 registers (CPU Timer1 & Timer2 re
CPU_TIMER2 : origin = 0x000C10, length = 0x000008 /* CPU Timer0 registers (CPU Timer1 & Timer2 re
PIE_CTRL : origin = 0x000CE0, length = 0x000020 /* PIE control registers */
PIE_VECT : origin = 0x000D00, length = 0x000100 /* PIE Vector Table */
DMA : origin = 0x001000, length = 0x000200 /* DMA Rev 0 registers */
MCBSPA : origin = 0x005000, length = 0x000040 /* McBSP-A registers */
MCBSPB : origin = 0x005040, length = 0x000040 /* McBSP-B registers */
ECANA : origin = 0x006000, length = 0x000040 /* eCAN-A control and status registers */
ECANA_LAM : origin = 0x006040, length = 0x000040 /* eCAN-A local acceptance masks */
ECANA_MOTS : origin = 0x006080, length = 0x000040 /* eCAN-A message object time stamps */
ECANA_MOTO : origin = 0x0060C0, length = 0x000040 /* eCAN-A object time-out registers */
ECANA_MBOX : origin = 0x006100, length = 0x000100 /* eCAN-A mailboxes */
ECANB : origin = 0x006200, length = 0x000040 /* eCAN-B control and status registers */
ECANB_LAM : origin = 0x006240, length = 0x000040 /* eCAN-B local acceptance masks */
ECANB_MOTS : origin = 0x006280, length = 0x000040 /* eCAN-B message object time stamps */
ECANB_MOTO : origin = 0x0062C0, length = 0x000040 /* eCAN-B object time-out registers */
ECANB_MBOX : origin = 0x006300, length = 0x000100 /* eCAN-B mailboxes */
EPWM1 : origin = 0x006800, length = 0x000022 /* Enhanced PWM 1 registers */
EPWM2 : origin = 0x006840, length = 0x000022 /* Enhanced PWM 2 registers */
EPWM3 : origin = 0x006880, length = 0x000022 /* Enhanced PWM 3 registers */
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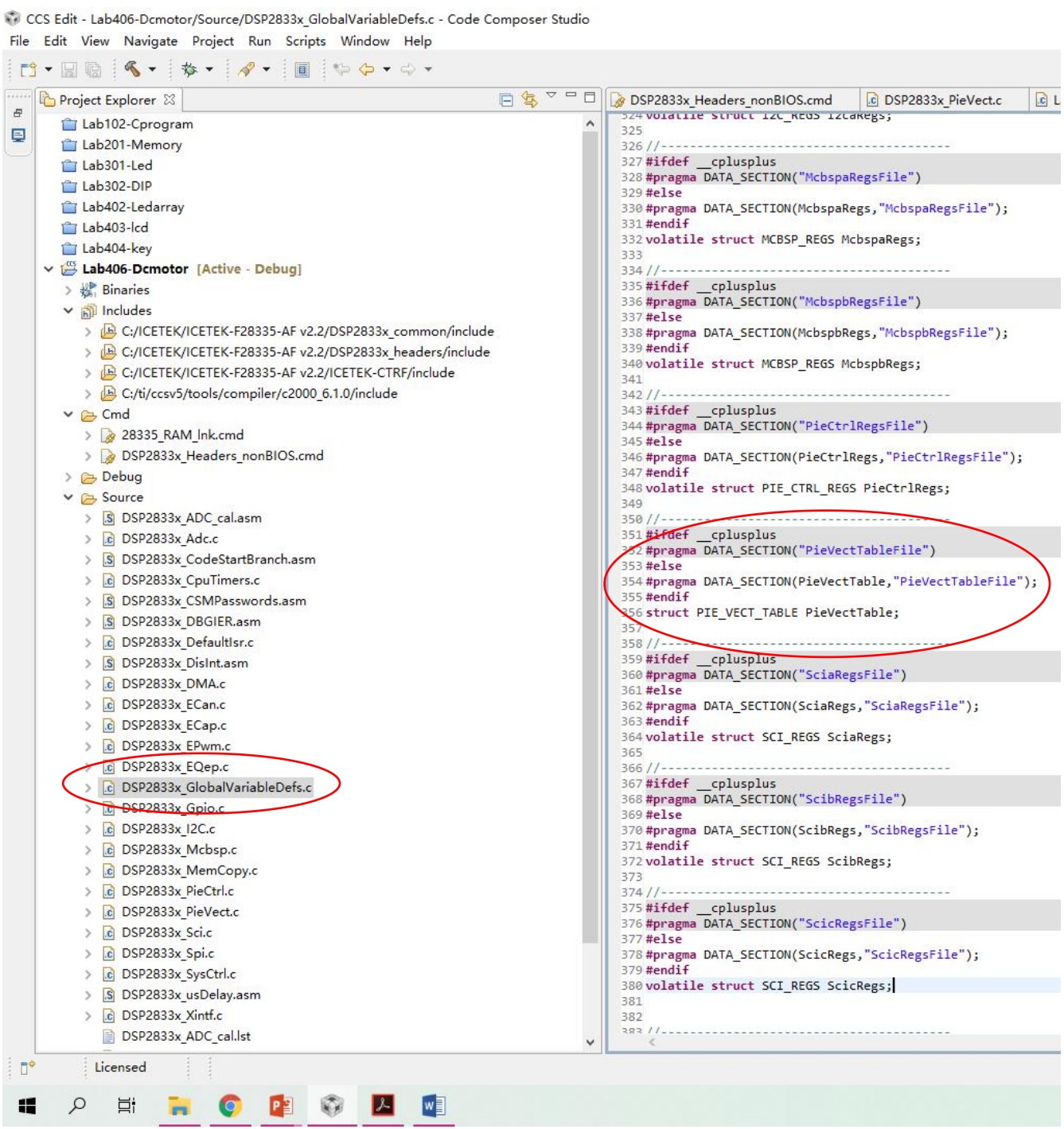
/Lab406-Dcmotor/Cmd/DSP2833x_Headers_nonBIOS.cmd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C:/ICETEK/ICETEK-F28335-AF v2.2/DSP2833x_common/include
C:/ICETEK/ICETEK-F28335-AF v2.2/DSP2833x_headers/include
C:/ICETEK/ICETEK-F28335-AF v2.2/ICETEK-CTRF/include
C:/ti/ccsv5/tools/compiler/c2000_6.1.0/include
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volatile struct I2C_REGS I2caRegs;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("McbspaRegsFile")
#else
#pragma DATA_SECTION(McbspaRegs,"McbspaRegsFile");
#endif
volatile struct MCBSP_REGS McbspaRegs;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("McbspbRegsFile")
#else
#pragma DATA_SECTION(McbspbRegs,"McbspbRegsFile");
#endif
volatile struct MCBSP_REGS McbspbRegs;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("PieCtrlRegsFile")
#else
#pragma DATA_SECTION(PieCtrlRegs,"PieCtrlRegsFile");
#endif
volatile struct PIE_CTRL_REGS PieCtrlRegs;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("PieVectTableFile")
#else
#pragma DATA_SECTION(PieVectTable,"PieVectTableFile");
#endif
struct PIE_VECT_TABLE PieVectTable;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("SciaRegsFile")
#else
#pragma DATA_SECTION(SciaRegs,"SciaRegsFile");
#endif
volatile struct SCI_REGS SciaRegs;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("ScibRegsFile")
#else
#pragma DATA_SECTION(ScibRegs,"ScibRegsFile");
#endif
volatile struct SCI_REGS ScibRegs;
//---------------------------------------
#ifdef __cplusplus
#pragma DATA_SECTION("ScicRegsFile")
#else
#pragma DATA_SECTION(ScicRegs,"ScicRegsFile");
#endif
volatile struct SCI_REGS ScicRegs;
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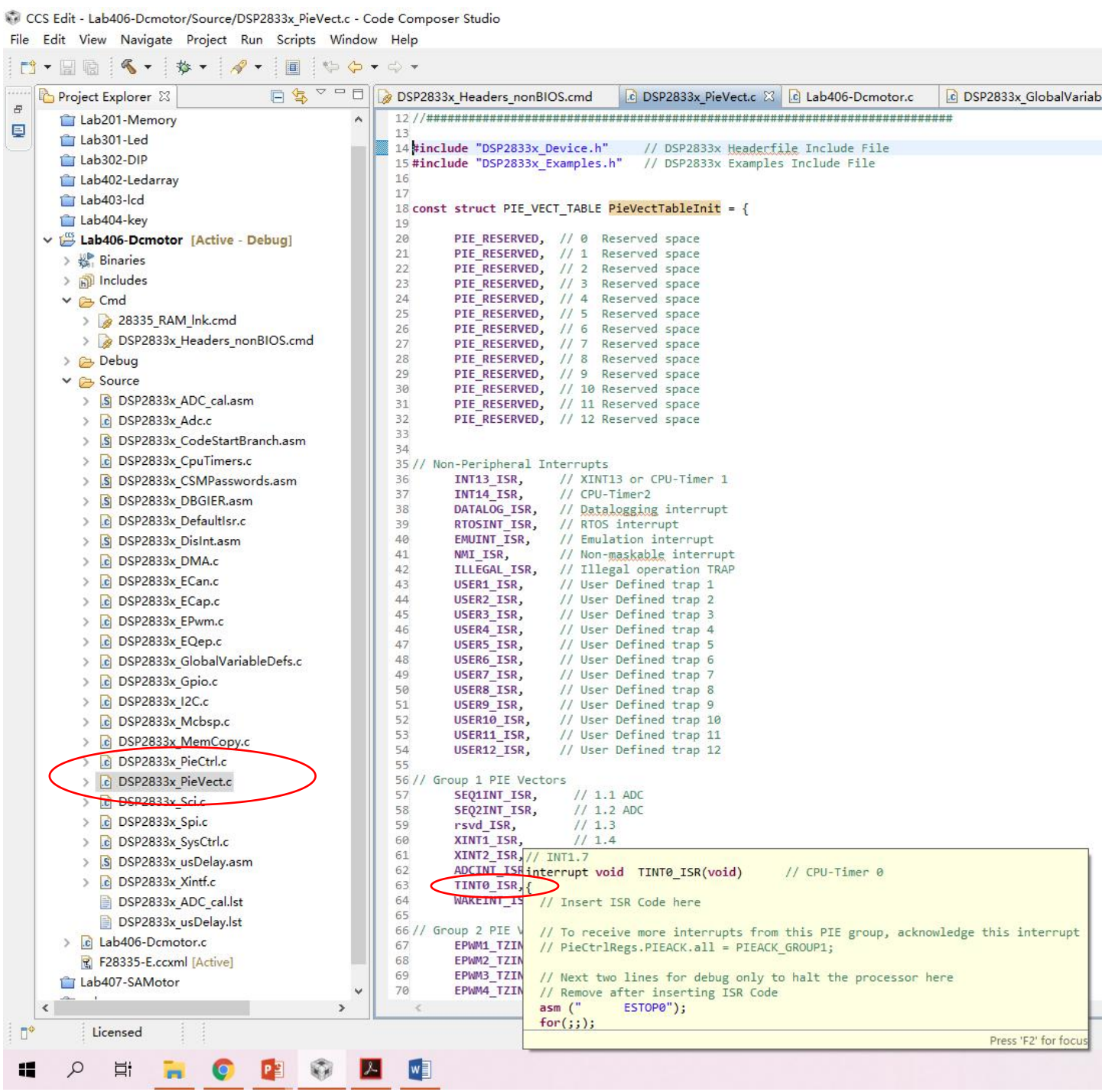
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DSP2833x_GlobalVariab
12 //###
13
14 #include "DSP2833x_Device.h"   // DSP2833x Headerfile Include File
15 #include "DSP2833x_Examples.h"   // DSP2833x Examples Include File
16
17
18 const struct PIE_VECT_TABLE PieVectTableInit = {
19
20   PIE_RESERVED, // 0 Reserved space
21   PIE_RESERVED, // 1 Reserved space
22   PIE_RESERVED, // 2 Reserved space
23   PIE_RESERVED, // 3 Reserved space
24   PIE_RESERVED, // 4 Reserved space
25   PIE_RESERVED, // 5 Reserved space
26   PIE_RESERVED, // 6 Reserved space
27   PIE_RESERVED, // 7 Reserved space
28   PIE_RESERVED, // 8 Reserved space
29   PIE_RESERVED, // 9 Reserved space
30   PIE_RESERVED, // 10 Reserved space
31   PIE_RESERVED, // 11 Reserved space
32   PIE_RESERVED, // 12 Reserved space
33
34
35 // Non-Peripheral Interrupts
36   INT13_ISR,   // XINT13 or CPU-Timer 1
37   INT14_ISR,   // CPU-Timer2
38   DATALOG_ISR,   // Datalogging interrupt
39   RTOSINT_ISR,   // RTOS interrupt
40   EMUINT_ISR,   // Emulation interrupt
41   NMI_ISR,   // Non-maskable interrupt
42   ILLEGAL_ISR,   // Illegal operation TRAP
43   USER1_ISR,   // User Defined trap 1
44   USER2_ISR,   // User Defined trap 2
45   USER3_ISR,   // User Defined trap 3
46   USER4_ISR,   // User Defined trap 4
47   USER5_ISR,   // User Defined trap 5
48   USER6_ISR,   // User Defined trap 6
49   USER7_ISR,   // User Defined trap 7
50   USER8_ISR,   // User Defined trap 8
51   USER9_ISR,   // User Defined trap 9
52   USER10_ISR,   // User Defined trap 10
53   USER11_ISR,   // User Defined trap 11
54   USER12_ISR,   // User Defined trap 12
55
56 // Group 1 PIE Vectors
57   SEQ1INT_ISR,   // 1.1 ADC
58   SEQ2INT_ISR,   // 1.2 ADC
59   rsvd_ISR,   // 1.3
60   XINT1_ISR,   // 1.4
61   XINT2_ISR,
62   ADCINT_ISR
63   TINT0_ISR,
64   WAKEINT_IS
65
66 // Group 2 PIE V
67   EPWM1_TZIN
68   EPWM2_TZIN
69   EPWM3_TZIN
70   EPWM4_TZIN
// INT1.7
interrupt void TINT0_ISR(void)   // CPU-Timer 0
{
  // Insert ISR Code here

  // To receive more interrupts from this PIE group, acknowledge this interrupt
  // PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;

  // Next two lines for debug only to halt the processor here
  // Remove after inserting ISR Code
  asm ("   ESTOP0");
  for(;;);
Press 'F2' for focus
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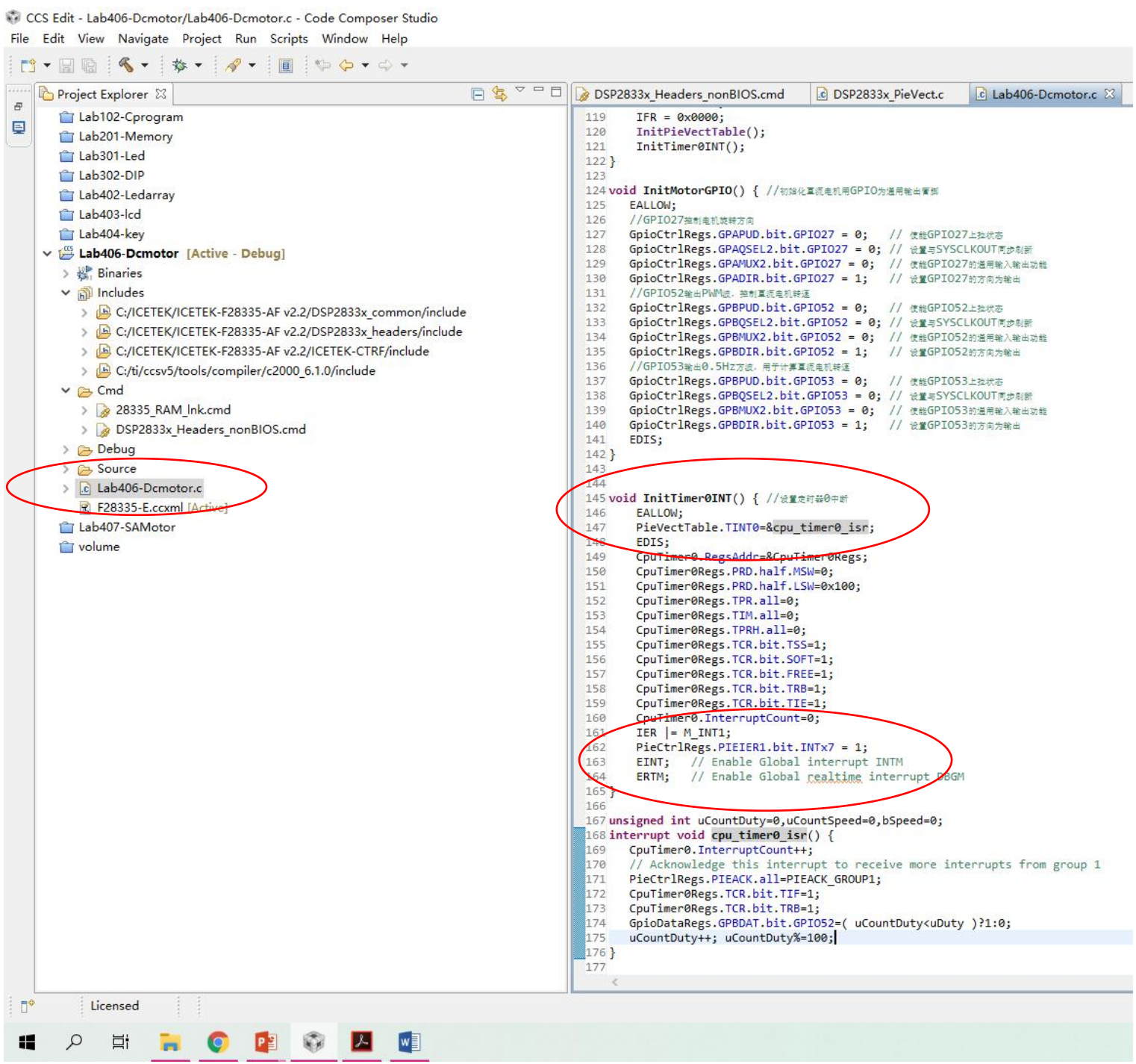
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Lab404-key
Lab406-Dcmotor [Active - Debug]
Binaries
Includes
C:/ICETEK/ICETEK-F28335-AF v2.2/DSP2833x_common/include
C:/ICETEK/ICETEK-F28335-AF v2.2/DSP2833x_headers/include
C:/ICETEK/ICETEK-F28335-AF v2.2/ICETEK-CTRF/include
C:/ti/ccsv5/tools/compiler/c2000_6.1.0/include
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DSP2833x_Headers_nonBIOS.cmd
DSP2833x_PieVect.c
Lab406-Dcmotor.c
IFR = 0x0000;
InitPieVectTable();
InitTimer0INT();
}
void InitMotorGPIO() { //初始化直流电机用GPIO为通用输出管脚
EALLOW;
//GPIO27控制电机旋转方向
GpioCtrlRegs.GPAPUD.bit.GPIO27 = 0; // 使能GPIO27上拉状态
GpioCtrlRegs.GPAQSEL2.bit.GPIO27 = 0; // 设置与SYSCLKOUT同步刷新
GpioCtrlRegs.GPAMUX2.bit.GPIO27 = 0; // 使能GPIO27的通用输入输出功能
GpioCtrlRegs.GPADIR.bit.GPIO27 = 1; // 设置GPIO27的方向为输出
//GPIO52输出PWM波，控制直流电机转速
GpioCtrlRegs.GPBPUD.bit.GPIO52 = 0; // 使能GPIO52上拉状态
GpioCtrlRegs.GPBQSEL2.bit.GPIO52 = 0; // 设置与SYSCLKOUT同步刷新
GpioCtrlRegs.GPBMUX2.bit.GPIO52 = 0; // 使能GPIO52的通用输入输出功能
GpioCtrlRegs.GPBDIR.bit.GPIO52 = 1; // 设置GPIO52的方向为输出
//GPIO53输出0.5Hz方波，用于计算直流电机转速
GpioCtrlRegs.GPBPUD.bit.GPIO53 = 0; // 使能GPIO53上拉状态
GpioCtrlRegs.GPBQSEL2.bit.GPIO53 = 0; // 设置与SYSCLKOUT同步刷新
GpioCtrlRegs.GPBMUX2.bit.GPIO53 = 0; // 使能GPIO53的通用输入输出功能
GpioCtrlRegs.GPBDIR.bit.GPIO53 = 1; // 设置GPIO53的方向为输出
EDIS;
}
void InitTimer0INT() { //设置定时器0中断
EALLOW;
PieVectTable.TINT0=&cpu_timer0_isr;
EDIS;
CpuTimer0.RegsAddr=&CpuTimer0Regs;
CpuTimer0Regs.PRD.half.MSW=0;
CpuTimer0Regs.PRD.half.LSW=0x100;
CpuTimer0Regs.TPR.all=0;
CpuTimer0Regs.TIM.all=0;
CpuTimer0Regs.TPRH.all=0;
CpuTimer0Regs.TCR.bit.TSS=1;
CpuTimer0Regs.TCR.bit.SOFT=1;
CpuTimer0Regs.TCR.bit.FREE=1;
CpuTimer0Regs.TCR.bit.TRB=1;
CpuTimer0Regs.TCR.bit.TIE=1;
CpuTimer0.InterruptCount=0;
IER |= M_INT1;
PieCtrlRegs.PIEIER1.bit.INTx7 = 1;
EINT; // Enable Global interrupt INTM
ERTM; // Enable Global realtime interrupt DBGM
}
unsigned int uCountDuty=0,uCountSpeed=0,bSpeed=0;
interrupt void cpu_timer0_isr() {
CpuTimer0.InterruptCount++;
// Acknowledge this interrupt to receive more interrupts from group 1
PieCtrlRegs.PIEACK.all=PIEACK_GROUP1;
CpuTimer0Regs.TCR.bit.TIF=1;
CpuTimer0Regs.TCR.bit.TRB=1;
GpioDataRegs.GPBDAT.bit.GPIO52=(uCountDuty<uDuty)?1:0;
uCountDuty++; uCountDuty%=100;
}
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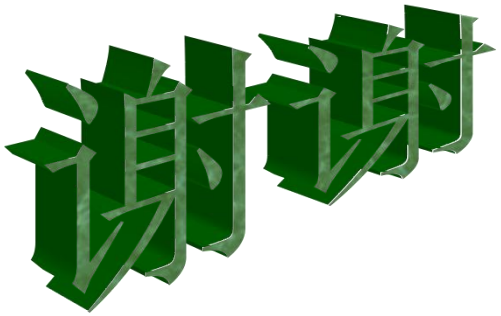
PIE中断向量表

Name	VECTOR ID [1]	Address [2]	Size (x16)	Description [3]		CPU Priority	PIE Group Priority
PIE Group 1 Vectors - MUXed into CPU INT1							
INT1.1	32	0x0000 0D40	2	SEQ1INT	(ADC)	5	1 (highest)
INT1.2	33	0x0000 0D42	2	SEQ2INT	(ADC)	5	2
INT1.3	34	0x0000 0D44	2	Reserved		5	3
INT1.4	35	0x0000 0D46	2	XINT1		5	4
INT1.5	36	0x0000 0D48	2	XINT2		5	5
INT1.6	37	0x0000 0D4A	2	ADCINT	(ADC)	5	6
INT1.7	38	0x0000 0D4C	2	TINT0	(CPU-Timer0)	5	7
INT1.8	39	0x0000 0D4E	2	WAKEINT	(LPM/WD)	5	8 (lowest)
PIE Group 2 Vectors - MUXed into CPU INT2							
INT2.1	40	0x0000 0D50	2	EPWM1_TZINT	(EPWM1)	6	1 (highest)
INT2.2	41	0x0000 0D52	2	EPWM2_TZINT	(EPWM2)	6	2
INT2.3	42	0x0000 0D54	2	EPWM3_TZINT	(EPWM3)	6	3
INT2.4	43	0x0000 0D56	2	EPWM4_TZINT	(EPWM4)	6	4
INT2.5	44	0x0000 0D58	2	EPWM5_TZINT	(EPWM5)	6	5
INT2.6	45	0x0000 0D5A	2	EPWM6_TZINT	(EPWM6)	6	6
INT2.7	46	0x0000 0D5C	2	Reserved		6	7
INT2.8	47	0x0000 0D5E	2			6	8 (lowest)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